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L1 and ((fail$4 adj3 input$4) and (fail$4 adj3 output$4))	1

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Search History

DATE: Tuesday, March 09, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=OR			
L5	l1 and ((fail$4 adj3 input$4) and (fail$4 adj3 output$4))	1	L5
L4	l1 and ((failsafe adj3 input$4) and (failsafe adj3 output$4))	0	L4
L3	l1 and ((failsafe adj3 input$4) and (falisafe adj3 output$4))	0	L3
L2	L1 and (telegraph or telegram)	9	L2
L1	(automat$3 adj system) and (input same output adj5 bus) and (fail$4)	225	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

L2: Entry 7 of 9 File: USPT Sep 18, 2001

DOCUMENT-IDENTIFIER: US 6292828 B1
TITLE: Trans-modal animated information processing with selective engagement

Brief Summary Text (4):
Surely tens of thousands of patents have been issued in the past 100-120 years in the telephony, radio, microwave, computer, cable, television, and electrical classifications. In recent years improvements have been made to telephony by the utilization of computer technology and the introduction of digital transmission, which is rapidly replacing analog transmission. Call waiting, call return, call forwarding, call blocking, and conference calling are but a few enhancements brought forth with the development of digital processing. These improvements, although laudable in their own right, fail to address the problems inherent in, say, running a household or a small business. More succintly, although considerable gains have been made in the respective and disparate fields of endeavor, very little has been done to enrich the American standard of living through notable advancement of communications fluency or safety standards.

Brief Summary Text (5):
In March, 1993 the American computer industry was still in the doldrums. In 1992, IBM had asked the federal government to intercede with financial aid. The telephone industry and Wall Street were getting ready for a slow summer in an aging bull market. The telephone industry was developing their land-line communication capabilities to include video transmission. The cable industry was preparing to be de-regulated, and busy with the development of two-way cable communication to compete directly with the phone companies. The Federal Communications Commission had announced that certain bands of the radio spectrum would be opened up for commercial use. Even electric utility providers were experimenting with the use of copper and alloy cables to eventually provide "spread-spectrum" signal communication capability through their systems. The respective players in this new and increasingly diverse communications arena were scrambling to develop their own products and services, wondering who would be the winners and losers on this new and crowded playing field. American Telephone and Telegraph's new Videophone and the EO Personal Digital Assistant had yet to reach the market. Apple's Newton Personal Digital Assistant was yet further away on the horizon. I felt that these tools had all somehow missed the mark. When the World Trade Center was bombed, I sensed an urgency to resolve some of our communication and security system shortcomings.

Brief Summary Text (32):
(q) to provide for user or system safety and integrity through alternate means of transmission for incremental enhancement, or in the event of failure or loss of any one medium;

Brief Summary Text (36):
Further objects and advantages of my innovation appear to be obvious when compared to previously existing prior art in communications and networking. For years now, those who carry portable phones have complained of the inherent lack of privacy in being "on call" at all times. With the impending onset of "500 channels" of the "information superhighway", many parents and authorities are becoming concerned that their families and children will be even more inclined toward a "couch potato"

lifestyle. Home and business alarm systems have been woefully inadequate and unreliable, with millions of dollars in losses occurring each year from false or failing alarms. Police departments all over the nation were being overwhelmed by alarm calls, and many had begun charging a fee for responses over a designated limit. Home communication systems have done little or nothing to promote interpersonal development between family members and loved ones. Communications networks in general had done little to facilitate dextrous or advantageous manipulation of available features. With the growing number of on-line computers and cellular phones, communications companies have a need for more effective management, routing, and monitoring of traffic. Business communication systems have been developing all too slowly, with too many missed or errant calls, and few intelligent operating system management tools. As recently as 1993, the telephone companies were struggling with the problems inherent in growth of metropolitan areas. It was reported that Atlanta would by necessity probably be split with another new area code being added soon. Conversely, now it has been announced that this, the nation's largest area code toll-free zone, will probably be approved for expansion by Mar. 1, 1994.

Detailed Description Text (4):
Central processing units and locally applicable peripheral monitoring, relay, control, utility, and communication devices may be located at fixed and/or mobile locations, including homes, businesses, vehicles, etc. These CPU's receive, store, and process inputs as warranted from wired or wireless on-site or off-site systems and non-systems stimuli, including other applicable receptors, servers, CPU's, broadcast media, etc. Optional multiplicity of wired or wireless communications media between locations insures continuity of, and provide asynchronicity of transfer, data, or communications between locations. These communications may be coded with identifications or other qualifications before or during broadcast or transmission. Monitoring at home, business, vehicle or other location, is typically performed by arrays of CPU's, microprocessors, transmitter/receivers, etc., from singularity of application, to complex multiple network topographies. Fixed or mobile monitoring or diagnostic routines may be performed continuously, at intervals, and/or on demand as dictated by system parameters and current, pre-set and/or anticipated events. Respective locations may provide or be subject to encryption based on user or system preferences or predetermined criteria. Respective locations may have reserve or alternate backup power source, and pre-programmed directives for data and equipment protection in case of main power supply failure. Individual, zone, and/or collective inputs to or between respective central processing units may be logged, assimilated, and/or analyzed for adherence to, or deviation from, acceptable levels of tolerance. Central processing units in multi-media entertainment broadcast facilities may broadcast or transmit data packets, or keys, which are embedded in the digitized programs. Upon recognition of incoming coded proposals for engagement of broadcasts or transmissions from on-site or off-site system or non-system components or devices, respective polled central processing units or microprocessors may analyze data keys or other qualifications for compatibility with system or user-defined acceptability, probability, volume indices, event sequence patterns, etc. Appropriate routines may be accessed, including return acknowledgments to polling CPU's, alternate reports as warranted to any system components, signals, alarms, or possible remedial actions as warranted. Remedial or terminal intervention and remedy of alarms or other system status may be possible either at or distant from interaction-monitoring location, as authorized by nascent priority schedules, conditions, or system configuration (s). Alternately, the polled CPU may be a component of a wireless portable receptor for incoming television or radio signal broadcasts, and equipped with a "quick-response triggers" apparatus. When notification of a proposed incoming "live" or predetermined reception is noted or recognized, the "quick-response triggers" apparatus of the polled unit may treat the proposal with the degree of authority allocated it during the ongoing period; or direct the signal reception or engagement to an appropriate on-site or off-site component for further evaluation or processing. Variables which may dictate the unit's nascent authority for

decision-making include user quick-format or extended programming formats, which may be programmed directly on the unit, or through wired or wireless relay from off-site or neighboring on-site user or system-authorized devices. Central processing units in respective locations, networks, etc., may relay data within or between individual devices or components to achieve desired results of incremental fluency and enhanced system efficacy. Thus the flow of data may be manipulated between devices and components, to achieve special effects such as scrolling, rewind, fast forward, or other advanced manipulatory regimen, etc. CPU's or other microprocessor-based devices including "quick-response triggers" apparatuses may assimilate, qualify, process, and manipulate data by means of comparison with reported inputs derived from other accessed microprocessors and applicable components. The user-friendly triggers apparatuses act as intelligence receptors, software-defined switches, and/or manipulatory output assistance devices, to allow enhanced management, data flow, tasking, and/or communications as necessary between components. Adjustments of parameters or switching of component tasking are performed by user or system components as warranted, including data transfer or accession to user or system-defined routines, including possible alarm status. Events are managed according to user or system inputs, priority schedules, system qualitative and quantitative analyses of events, conditions, or interactions (or lack thereof) between system or non-system components and devices. System integrity may be enhanced by selective electronic prequalifications, and progressive cognitive and interrogatory routines. Formulative conclusions or advanced routines may be engaged, according to qualifications and prioritizations, with predetermined, designated, or errant events or conditions accessing alternate components or routines, including possible local, system-wide, or site-specific alarm status. Authorized users, callers, or devices accessing system-related CPU's and components may be appointed discreet or human-voice options, or other user-friendly methods for manipulation of choices. Coded, nuanced, or directly postulated or associated signal qualities may be employed for engagement routine (s). Custom tailoring of programs, messages, routines, parameters, coding, etc., may be formulated with appropriate responses to menu selections by users or system-authorized devices, including "quick-response triggers" apparatuses. Alternate routines may also be dispatched from and/or through triggers devices or other authorized locally applicable system or non-system equipment with appropriate responses to menus as presented. Historic, current, and/or anticipated events, conditions, and interactions may be recorded, stored, processed, coded as possible, and appropriate routines accessed. Formulation of individual databases derived from historic events may be developed, and automated remedial interactions generated between applicable components as necessary. outgoing wired and/or wireless communications transmissions may be relayed by modems or other devices, including bridging and routing equipment, according to system or device parameters and relevant interactions considerations. Communications may be forwarded to authorized locations as dictated by user or system specifications and parameters, signals, controls and ongoing interactions. Individual, zone, and/or collective notifications of historic, current, or anticipated events, as well as notifications of impending degree(s) and qualities of coded voice, video, and/or other transfers or transmissions may be thus dispatched to such locations as are authorized by the user or system to receive transfers or communications from the transmitting devices or components. This may be facilitated by deployment of transmissions through locally feasible, applicable, and appropriate wired and/or wireless communication or power transfer channels, whether analog, digital, spread-spectrum, etc. Multiple transfer or communications media are most efficacious, offering extended versatility, functionality, continuity, and safety to the system as well as components and users. Communications may be forwarded to and/or through locations of authorized on-site and off-site fixed or mobile system or non-system relay components and terminal devices, including "triggers"-equipped devices and components. "Triggers"-equipped components by definition are equipped for quick-response acknowledgments, return notifications, queries, or commands to or from respective polled or polling components, in real-time or system-compatible parameters; typically comprising degree(s), nature(s), and/or other qualifications

as necessary, of intended forthcoming or proposed event(s) or interaction(s). Thus, respondent notification by use of "quick-response" manual, voice-driven, and/or electronic "triggers", may apprise applicable system components of a range of intended interactions such as: (a) deferred or delayed interaction; (b) limited, qualified, or intermediate interaction; (c) full or formulative interaction by users and devices. Upon signalling from incoming broadcasts, communications, or transmissions, the "triggers"-equipped system component may be notified of the source, type, quality, volume, etc., of incoming transmissions by appropriate coded signalling respective to parameters. These signalling means may comprise visual, audible, or electronic notifications or manipulation(s) relative to parameters. Audible or visual signalling may be in the form of industry-standard lighted or graphic displays, tonal variations, or other signalling in terms relative to parameters. Custom-tailoring of programs, messages, routines, parameters, displays, etc., may be executed with appropriate selection(s) from menu items available in either the CPU at the originating location, or through the quick-response apparatus or other locally applicable user or system-authorized system or non-system device (s). Inputs, pre-determinations of interactive availability, and commands may be stored in a quick-response apparatus during a period of detente, until appropriate receptor is available for consummation of the interaction. Electronic, audible or visual prompts may notify the user or system of progressive or predetermined events consummations. The signalling means may also include signalling and control of electrically or electronically-activated devices and components, as deemed appropriate and locally applicable, through authorized relay devices. Data, transfers, or actions relevant to electrical power usage, control, management, etc., may be forwarded through authorized on-site or off-site system or non-system components as warranted by conditions. An electrical network monitoring apparatus with optional database may be employed at individual site(s) to collect, analyze, disperse, or manipulate indications or notifications which occur in individual, zone, or collective circuits, locations, etc.

Detailed Description Text (9):
Conditions requiring intercessory assistance may include such errant events as the attempted downloading of a movie with a non-homogeneous rating, or peripheral introduction of other intrusive data such as home-based security alarm conditions. Notification of these or any conditions, including incoming personal communications, may be forwarded to one or more on-site or off-site terminal or remedial remote stations for constructive deliberation, as dictated by cognizance and availability, for acceptance or denial of the action or offering. Of course, this same method can be used to carry on an extended virtual dialogue with the H.E.N., or to send or receive discreet interval reports or directives, with selective monitoring. A problem arises, however, when the stream of reported data increases to overwhelming proportions in terms of interaction frequency or flow, or inaccessibility of the user to react immediately to the polling unit. The "quick-response triggers" device or apparatus, however, with its singular or multiple array of manually-deployed ergonomically-efficient buttons, or electronic or acoustic triggers, enables the user to promptly signal the polling station (or other applicable components) of the availability of the user or polled device. Identifications and qualifications of the polling device or party are intelligently formulated and routed to the "triggers"-equipped apparatus. Entire routines or menus may be forwarded; or pre-programmed compatible routines may be retained in the storage component of the "quick-response triggers" apparatus. In the event of user absence or other unavailability for interaction, the "triggers" apparatus may respond with appropriate return or alternate notifications. These responses may include such information as the device or component is equipped to store or process. Responses may range from user-defined or system-defined pre-set electronic responses or verbal greetings, to device or system-calculated reports or engagements. Advanced routines may signal other distant or neighboring system-authorized components or devices, to enable further versatility or formulations. Advanced configurations may incorporate modular jacks for direct-wired relay to other components. Configurations may incorporate multiple transmitter/receivers and

multiple microprocessors for intelligent switching and formulative solutions to multiple transactions. In the favored configuration for remote on-site or off-site monitoring of the H.E.N., a hand-held or pocket-oriented device or phone may be equipped for radio or other wireless communications, as well as modular jacks for land-line deployment as necessary or available. This hand-held device may be equipped with one or more of the "quick-response triggers" apparatuses as necessary. A "triggers" apparatus may be housed in a smaller hand-held configuration which manages the interactions of some or all of the neighboring system-authorized components, through wired or wireless relay application. Thus, this smaller device may be less unwieldy, and allow flexible application through neighboring system-authorized components whether at a fixed or mobile location. The transmitter/receiver and microprocessor components may be modular, to allow ease of replacement to adjust to changing system configurations of the particular user. The "triggers" apparatus may be incorporated within any communication or broadcast reception device, including home-based or portable multi-media reception devices. In the manually-driven quick-response triggers array, three buttons may be arranged in a cluster which may be conveniently located for quick accessibility. One button may be programmed to signal the system or caller of a deferred or delayed interaction. The next button may signal the system or caller of an intermediate, limited, or qualified interaction. Either of these buttons may be pre-programmed or re-programmed to trigger alternate routines which further signal the system or caller with such notifications as "estimated time of delay". The third button may signal the system or caller of full or formulative response, including such other system-defined information designed to enhance efficacy. This array can be fully appreciated in heavy traffic or in intense business situations, where even routine incoming calls on a portable phone can be distractive and inconvenient. The manipulative array of buttons of the quick-response apparatus allows discreet and judicious interaction of the user according to his or her availability. Selection can be made from the "interactive availability menu" without taking one's eyesight and attention away from the roadway ahead, or while the unit is held out of sight under a table or in a coat pocket, for example. Deferred or delayed interactions may result in accession to alternate or advanced routines, including designated outgoing messages which may correspond to recognition of incoming caller, time of day, priority schedules, etc. These alternate messages may be pre-programmed or field-programmed, dispatched as voice mail to a caller, etc. The "detente" feature increases the fluency and independent functionality of the system and user, by accepting and recording audible and other inputs, and storing them until a polled receiving station is ready, for example. Virtual dialogue, control of system and devices, or reprogramming of parameters may be accomplished with minimum of effort through intuitive and informative qualities of detente commands and responses. The detente feature may also be used for manipulation of programs, error correction or reduction, and management of flow in ongoing interactions, such as automated switching, transfer, and flow regulation, and other enhanced directives. For example, a digitized movie, song, or recorded message may be "forwarded" or "reversed" at user or system will, through intelligent manipulation of the digitized data stream in and through networked monitoring components in an application. Flexibility and reliability of portable wireless quick-response components and other components may be enhanced by optional hard-wired application through modular jacks, receptacles, etc. Integrity of the quick-response apparatus and other system components is enhanced by the use of advanced routines and alarms upon discovery of errant conditions. Reserve or alternate power sources may be accessed by the user(s) or system devices, in the event of power failure. Variations of many features which are described above for use in remote devices to monitor the home enhancement network are inherent in or applicable to the monitored location H.E.N. or B.E.N., etc.

CLAIMS:

4. A system as set forth in claim 1, further comprising means for automated system processing of events or conditions, wherein said detected events or conditions are

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presented to one or more general-purpose memory units in one or more programmable logic devices at one or more component locations.

7. A system as set forth in claim 1, further comprising means for indication of said detected conditions to be forwarded to or from integral input/output device, by appropriate bus device or direct interconnection, to or from circuits comprising one or more of the following types:

(1) transducer circuits,

(2) detector circuits,

(3) amplifier circuits,

(4) oscillator circuits,

(5) modulation or demodulation circuits,

(6) relay circuits,

(7) filter circuits,

(8) buffer circuits,

(9) volatile or non-volatile memory circuits, or

(10)) programmable logic circuits.

L1: Entry 84 of 225 File: USPT Jun 20, 2000

DOCUMENT-IDENTIFIER: US 6079033 A
** See image for Certificate of Correction **
TITLE: Self-monitoring distributed hardware systems

Detailed Description Text (5):
more peripheral devices (not shown). The functions of host systems 102, 104, and 106 can be varied, depending on the environment in which network system 100 is placed. In one embodiment, host systems 102, 104, and 106 can share processing of applications, share data, and control the same or different peripherals. Examples of environments into which network system 100 can be placed include single-family homes, multi-family dwellings, offices, industrial settings, toll collection facilities, and space stations. Additionally, in one embodiment, network system 100 is coupled to various electronic components in an individual residence, including one or more of the entertainment system(s), security system(s), and home automation system(s).

Detailed Description Text (56):
FIG. 6 illustrates a hardware system or machine suitable for use as a host or server system according to one embodiment of the present invention. In one embodiment, host systems 102, 104, and 106, as well as server system 108 illustrated in FIG. 1 are each a hardware system 600 of FIG. 6. In the illustrated embodiment, hardware system 600 includes processor 602 and cache memory 604 coupled to each other as shown. Additionally, hardware system 600 includes high performance input/output (I/O) bus 606 and standard I/O bus 608. Host bridge 610 couples processor 602 to high performance I/O bus 606, whereas I/O bus bridge 612 couples the two buses 606 and 608 to each other. Coupled to bus 606 are network/communication interface 624, system memory 614, and video memory 616. In turn, display device 618 is coupled to video memory 616. Coupled to bus 608 is mass storage 620, keyboard and pointing device 622, and I/O ports 626. Collectively, these elements are intended to represent a broad category of hardware systems, including but not limited to general purpose computer systems based on the Pentium.RTM. processor, Pentium.RTM. Pro processor, or Pentium.RTM. II processor manufactured by Intel Corporation of Santa Clara, Calif.

Detailed Description Text (64):
The instructions are copied from the storage device, such as mass storage 620, into memory 614 and then accessed and executed by processor 602. In one implementation, these software routines are written in the C++ programming language. It is to be appreciated, however, that these routines may be implemented in any of a wide variety of programming languages. Thus, it can be seen that the wellness token can only be verified and modified correctly if processor 602, cache 604, host bridge 610, bus 605, and system memory 614, as well as possibly additional devices, of hardware system 600 are functioning properly. Over time, failure by any of these components will most likely cause a failure in the verification and modification of the wellness tokens, thereby allowing performance of system 600 to be verified as opposed to, for example, simply network/communication interface 624.

L1: Entry 81 of 225 File: USPT Aug 14, 2001

DOCUMENT-IDENTIFIER: US 6275881 B1
TITLE: Device for inherently safe signal matching

Abstract Text (1):
The invention relates to a device for an inherently safe signal matching of signals being exchanged between an automating system (2) and field devices (3). The device (1) contains input/output modules (4), which can be plugged into a backwall plate (19) and which combine the functions of conventional input/output modules and modules for voltage separation. The backwall plate (19) supports data lines (20) of a local bus (8), as well a current supply lines (21). A communications module (9) is connected on the one hand with the local bus (8), and on the other hand with a field bus (12). The communications module (9) contains device, for memorizing (22) and processing (16) data, and makes possible an asynchronous data exchange between an automating system (2) and the input/output modules (4).

Brief Summary Text (2):
The invention relates to a device for an inherently safe matching of signals and more specifically to a device that allows the safe and efficient exchange of input/output modules within an automating system.

Brief Summary Text (3):
Such a device is known from WO 92/04813. Such a device for an inherently safe signal matching is intended to provide a safe separation, in the sense of an explosion protection, of the signal flow between an automating system and so-called field devices, i.e. sensors and actuators, in connection with an explosion-endangered process.

Brief Summary Text (4):
With the known device, a number of input/output modules can be plugged into a backwall plate with an assembly rail. These input/output modules are connected by means of a communications unit, also plugged into the assembly rail, with a computer of the automating system, wherein the setting of parameters and the initialization of the device takes place directly by the automating system.

Brief Summary Text (5):
This applies in the same way for performing a diagnosis, which is also performed directly by the automating system.

Brief Summary Text (8):
The device in accordance with the invention operates with input/output modules, which are connected via a communications module with devices for data processing and data storage with the automating system via a field bus. By means of this, and by means of at least one further standard interface connected with the communications module, it is possible to store and recall parameters for the initialization and automatic configuration of the device in accordance with the invention in the communications module, safely in case of a current supply net failure. Furthermore, the setting of parameters performed by the communications module, in particular with the modular construction of the backwall plate, furthermore is used for an easier adaptation of the device in accordance with the invention, for example in case of the removal of this device.

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Detailed Description Text (3):
FIG. 1 shows a device 1 for the inherently safe matching of the signals to be exchanged between an automating system 2 and field device 3, wherein primarily the paths of the signal flow are represented. The device 1 contains a plurality of input/output modules 4 with I/O connectors 5 for the field devices 3. The input/output modules 4 contain a local bus interface 6 and are connected via a contacting device 7 with lines 20 (FIG. 2) of a local bus 8.

Detailed Description Text (4):
The device 1, furthermore, contains a communications module 9, which also has a local bus interface 6 and a contacting device 7 for connection with the local bus 8. The communications module 9 has a field bus interface 10 and a field bus connector 11. The device 1 is connected via the field bus connector 11 with an automating system 2 via a field bus 12. The field devices 3 are respectively connected via lines 13 with the I/O connectors 5. In a possible structural embodiment explained further down below by means of FIG. 5, the field bus connector 11 is located on an initial plate 19.1 instead of on the module 9.

Detailed Description Text (5):
The automating system 2 can be, for example, a memory-programmable control. Digital or analog sensors or actuators can be connected as the field devices 3. The contacting device 7 can be a plug connection or an arrangement of pressure contact pins, for example. The local bus 8 is preferably embodied as a simple, serial and cost-effective bus. Control of the local bus 8 can take place from the communications module 9.

Detailed Description Text (7):
FIG. 3 shows further details of the communications module 9. Besides two microprocessors 16, the module 9 contains a memory 22. Besides the local bus interface 6 and the field bus interface 10, standard interfaces 23, 24 are also provided (for example, RS 485), which are used for setting parameters (for example by means of a PC or a local display and operating unit with manufacturer-specific and HART protocol). All parameters can be stored in the communications module 9 safe against failure of the current supply net, and are transmitted to the I/O modules 4 in the initialization phase. It can be furthermore seen from FIG. 3, that a redundant auxiliary energy input from redundant current supply strip conductors 21 can be provided, for example, if more than eight input/output modules 4 are used.

Detailed Description Text (11):
The device 1, represented in FIGS. 1 to 5, makes possible the conversion of analog signals of the field devices 3 in the input modules 4 into digital values. Data transmitted via the local bus 8 to the communications module 9, the same as configuration and status information, are intermediately stored there in accordance with a memory map method. Thus the communication module 9 permits an asynchronous connection with the automating system.

Detailed Description Text (12):
The system is self-configuring, so that neither address switches nor external aids or respectively software are required in order to fix the function or position of individual modules. Input/output modules 4 are allowed to be exchanged while charged with voltage, while the remaining modules continue to work free of interference. All parameters, for example for temperature ranges, threshold values and error recognition are stored, safe against loss of the current supply net, in the communications modules and can be called up by means of the standard interface 24 for a PC connection. Setting of parameters can take place from the automating system 2 as well as via the standard interface 24.

CLAIMS:

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1. A device for the inherently safe signal matching of signals being exchanged between a system and field devices comprising:

a backwall plate, dividable into individual plates, which supports data lines of a local bus and current supply lines;

input/output modules having a local bus interface, a data processing device and a signal matching device, which can be attached to said backwall plate via connections; and

a communications module, attached to said backwall plate, having a local bus interface which is connected to a field bus interface, a data processing device and a memory for storing parameters obtained via an interface for setting parameters for the input/output modules.

9. A device for the inherently safe signal matching of signals being exchanged between an automating system and field devices, the device comprising:

a backwall plate having an initial plate and adjacent modular plates, the backwall plate supporting data lines of a local bus and current supply lines;

input/output modules connected to the backwall plate, each input/output module having a data processing device, a signal matching device, and a local bus interface for connection to the local bus; and

a communications module connected to the backwall plate, the communications module having a local bus interface connected to a field bus interface, a processor, and a memory for storing parameters obtained via an interface for setting parameters for the input/output modules.

12. The device of claim 9 wherein the memory of the communication module stores initialization parameters and the initialization parameters are transferred to the input/output modules upon the input/output modules making contact with the local bus.

13. A modular interconnect apparatus for communicating signals between an automating system and field devices, the apparatus comprising:

a backwall plate having an initial plate and at least one modular plate interconnected to the initial plate, the backwall plate defining a local bus having a data line and a current supply line;

at least one input/output module connected to the modular plate, the input/output module having a processor, a signal matching device, and a local bus interface for connection to the local bus; and

a communications module connected to the backwall plate and interconnecting the initial plate with the modular plate, the communications module having a local bus interface electrically connected to a field bus interface, a processor, and a memory for storing parameters obtained via an interface for initializing the input/output modules.

17. The apparatus of claim 13 wherein the parameters stored in the memory are transferred to the input/output module upon the input/output module making contact with the local bus.

L2: Entry 8 of 9 File: USPT Jul 7, 1992

DOCUMENT-IDENTIFIER: US 5128855 A
TITLE: Building automation system operating installation control and regulation arrangement

Abstract Text (1):
An arrangement for the control of an operating installation of a building automation system is disclosed. The arrangement comprises a control module serving as a master transmitter-receiver and at least one function module serving as a slave transmitter receiver. A bus connection including a bus rail connects the control module and the at least one function module for the transmission of addresses and data and for the transmission of operating voltages. The bus rail is installed electrically at the periphery of the installation so that the at least one function module is connected to a plurality of conductors forming the bus rail and directly to the installation so that the function module serves as an input/output terminal of said installation for the transmission of process parameters.

Brief Summary Text (2):
The instant invention relates to an installation for the supervision, control and regulation of a technical operating plant of a building automation system.

Brief Summary Text (12):
The concept of a technical operating plant comprises all the power current, hydraulic and pneumatic installations of an automation system of a building, including their control and answerback communication elements, but not including the actual control and answerback signals. The control and answerback communication elements are here sensors, e.g. temperature and/or pressure sensors, servo components for e.g. mixing valves and/or motors of pumps, compressors, blower-burners and aerators, or control elements comprising, for example, safety coils and answerback communication contacts.

Brief Summary Text (18):
In the periodical "Landys & Gyr Mitteilungen", 26th year (1979) 1-79, pages 2 to 12, "Visonik-ZLT-System", P. Schneider and J. B. Lumpert, as well as in the brochure "Building Management Systems, Introduction to the Visogyr/Visonik System Family", Aug. 1987, order no. ZXGU 0100D, Landis & Gyr, CH 6301 Zug, Switzerland, a ZLT Building Automation System based central management technology for the realization of these requirements is described, making it possible to connect a central station via a multi-wire ring circuit by means of transmission technology to several sub-systems designated as sub-stations. All control and message devices of a sub-system are in this case located in one control cabinet or control panel.

Brief Summary Text (19):
In this known ZLT building automation system a bus rail is used. The structure of this bus rail is described in the patent GB-PS 2,014,367. This bus rail constitutes within the ZLT building automation system an electric bus connection between a control module and several function modules of one and the same sub-system and contains a plurality of parallel electric conductors insulated from each other, i.e. 33 conductors, for the parallel multibit transmission of addresses and digital values, each via a separate bus, as well as for the analog transmission of analog

values and supply voltages. A conversion of the analog values into digital values takes place relatively slowly only in a first central computer within and/or outside the control module, so that the computer is occupied for a relatively long period of time with conversion tasks for this purpose. The positions in which the individual function modules are installed are provided with encoded addresses so that the individual function modules can be located only in very precise positions without hardware and/or software changes

Brief Summary Text (21):
It is the object of the instant invention to change the known ZLT building automation system while improving its advantages as much as possible in such manner that an even more universal ZLT building automation system may be created, in which wiring, terminals, connection and assembly costs within the control cabinet or control panel are reduced to a minimum and in which no expensive jumper wiring is necessary since the connections of the technical operating plant are not connected to isolated terminals but directly to base terminals of the function modules in order to realize great economies in money and in time.

Brief Summary Text (23):
The present invention is an arrangement for the control of an operating installation of a building automation system. The arrangement comprises a control module serving as a master transmitter-receiver and at least one function module serving as a slave transmitter-receiver. A bus connection including a bus rail connects the control module and the at least one function module for the transmission of addresses and data and for the transmission of operating voltages. The bus rail is installed electrically at the periphery of the installation so that the at least one function module is connected to a plurality of conductors forming the bus rail and directly to the installation so that the function module serves as an input/output terminal of said installation for the transmission of process parameters.

Brief Summary Text (28):
a reduction of the number of failure sources due to the fact that the start-up and testing of the installation in order to find any wiring errors is simplified,

Drawing Description Text (2):
FIG. 1 shows a known installation for the supervision and the control of a technical operating installation of a building automation system,

Drawing Description Text (26):
FIG. 25 shows a block diagram of an output circuit of a third variant of the function module, of a data telegram,

Drawing Description Text (28):
FIG. 27 shows a symbolic representation of a reading cycle of a data telegram,

Detailed Description Text (2):
In order to promote a better understanding of the difference between the invention and the above-mentioned state of the art, the known ZLT building automation system is shown once more in FIG. 1.

Detailed Description Text (4):
Binary data are preferably frequency-modulated, e.g. transmitted by means of frequency shift keying (FSK) in one direction from the output of the computer 1 via the ring circuit 6 and the control modules 10 to the input of the computer 1. The data flow is represented symbolically in FIG. 1 by wide arrows. Commands are for example transmitted in form of messages N1 and N2 from the computer 1 to the first or third sub-system 7, and the corresponding message receipts QN1 or QN2 are then transmitted from the first or from the third sub-system 7 to the computer 1. Furthermore, the events E1 and E2 representing the state changes in the technical

operating installations 9 of the corresponding sub-systems 7 are transmitted from the second or third sub-system 7 to the computer 1. The transmitted data telegrams are secured with a cyclic redundancy code (CRC). If transmission errors occur, the existence of an error is acknowledged and the transmitted data telegram in question is repeated.

Detailed Description Text (5):
All control modules 10 are structured identically and, in the known ZLT building automation system, each contains among other things a frequency demodulator, a frequency modulator, a micro-computer, an analog/digital converter as well as an input device for the electronic strip terminal 8. Each control module 10 contains furthermore a "watchdog" circuit for self-monitoring When the self-monitoring system comes into action, this is displayed on the corresponding control module 10 and is printed out on a printer 5. Indicators for the self-monitoring system as well as jacks for the connection of a local operating device (not shown) are located on the face plates of the control modules 10. The control module 10 of each sub-system 7 controls and monitors in a fully independent manner all the data exchange within its electronic strip terminal 8 for its zone, but also to its local operating device and to the computer 1.

Detailed Description Text (12):
In the building automation system according to the invention the central station 1; 2; 3; 4; 5 and the ring circuit 6 need not necessarily be structured as shown in FIGS. 1 and 2 but can be realized also in some other manner.

Detailed Description Text (40):
The control module 10 is interrupt-active and operates entirely autonomously under the control of the microcomputer 50 in order to exchange a binary telegram with the function modules 11. The manner of operation of the microcomputer 50 and its auxiliary circuits are described in detail in the documentation of the Motorola company. In the time-multiplex process, the bus linkage 55 contains either address or data which are demultiplexed under the direction of the microcomputer 50 in the following manner. The addresses are loaded with each leading edge of the AS signal into the flipflop 52a of the address register 52 where they are stored. Simultaneously, when the R/W or the E signal is low so that the AND gate 54a is locked, the RS flipflop 54b is reset to zero by the AS signal, i.e. a logic value "0" appears at the output of the NOR gate 54c, causing the drivers 53c to be locked and the drivers 53b to be freed. The data driver 53 is thus switched into the direction of transmission. When the microcomputer wants to initiate a writing cycle it gives a logic value "0" to the R/W signal and this confirms the momentary status of the RS flip flop 54b since the AND gate remains locked. The data driver 53 thus continues to be switched into the direction of transmission as desired. If on the other hand a reading cycle is initiated by the microcomputer, it assigns the R/W signal a logic value "1", causing the RS flipflop to be changed over with the next leading edge of the E signal since the output signal of the AND gate 54a then assumes a logic value "1". The switching over of the RS flipflop 54b causes a logic value "1" to appear at the output of the NOR gate 54, causing drivers 53c to be released and the drivers 53b to be locked so that the data driver 53 is switched into direction of reception, as desired. The R/W signal of the microcomputer 50 thus determines by means of the E signal and of the directional control device 54 whether the data appearing at the "C-Port" of the microcomputer 50 are carried from the C-port via bus linkage 55, drivers 53b of the data driver 53 and data bus 57 to the interface circuit 21 or vice-versa, whether the data supplied by the interface circuit 21 are transmitted via data bus 57, the drivers 53c of the data driver 53 and the bus linkage 55 to the C-port of the microcomputer 50.

Detailed Description Text (41):
The interface circuit 21 of the control module 10 shown in FIG. 8 comprises an address register 58, a function register 59 in case that a function byte is to be transmitted, of at least one data register 60 or 61, of a status register 62, a

verification device 62a serving as a control device, a shift register 63, a monitor-error detector 64, an invertor 64a, a multiplexer 65a, a CRC generator 65b, an OR gate 65c, a transmission unit 66 and an AND gate 67 which serves as a receiving unit. The multiplexer 65a, the CRC generator 65b and the OR gate 65c are only present if a CRC byte is to be transmitted and evaluated. Preferably two data registers 60 and 61 are used as is assumed hereinafter, since preferably also two data bytes are transmitted in the data telegram. The bus 56 is connected to one bus input of each of the five registers 58 to 62. Similarly, bus 57 is connected to a first bus connection of each of the five registers 58 to 62. One bus link 68 with preferably 8 bus conductors connects a second bus connection of each of the four registers 58 to 61 to a parallel input-output with 32 bits of the shift register 63 the serial output of which is connected by a single pole to an input of the transmission unit 66. The shift register 63 is a 32-bit shift register and all four bus connections 68 together constitute a 32-bit bus. The output of the AND gate 67 is connected to a first input of the multiplexer 65a and to a serial input of the shift register 63. The output of the multiplexer 65a is connected to a signal input of the CRC generator 65b and its parallel outputs are connected to the inputs of the OR gate 65c. One output of the monitor-error detector 64 and one output of the OR gate 65c is connected to one input of the status register 62. The transmission unit 66 has a NAND gate 66a, an invertor 66b, a flipflop 66c and a NAND gate 66d. The D input of the flipflop 66c constitutes the input of the transmission unit 66, the clock input of which, which is furthermore connected to the input of the invertor 66b, is constituted by the clock input of the flipflop 66c. The output of the invertor 66b is connected to a first input of the NAND gate 66a, the second input of which constitutes a first control input and the output of which constitutes a first output of the transmission unit 66. The inverted Q output of the flipflop 66c is connected to a first input of the NAND gate 66d, the second input of which constitutes a second control input and the output of which constitutes a second output of the transmission unit 66. Each of the two outputs of the transmission unit 66 is connected to the conductor 29 or 31 of the bus 22 while its conductors 33 are each connected to a first input of the AND gate 67 and of the monitor-error detector 64. The output of the NAND gate 66d is furthermore connected to a second input of the monitor-error detector 64 and to one input of the multiplexer 65a. A first control output of the verification device 62a at which an EC (enable clock) signal appears is connected to a first control input and a second control output of the verification device 62a at which an ES (enable send) signal appears is connected to the second control input of the transmission unit 66. The second control output of the verification device 62a is furthermore also connected to a control input of the monitor-error detector 64 and to a control input of the multiplexer 65a. A third control output of the verification device 62a at which an ER (enable reception) signal appears is connected to a second input of the AND gate 67 and to a control input of the CRC generator 65b. A reset output of the verification device 62a at which a reset CLR (clear) signal appears is connected to a reset input of the transmission unit 66, to a reset input of the monitor-error detector 64 and to a reset input of the CRC generator 65b, with the reset input of the transmission unit 66 being constituted by the reset input of the flipflop 66c. A clock output of the control device 62a, at which a CLK (clock) signal appears, is connected to a clock input of the transmission unit 66, to one input of the CRC generator 65b and (via invertor 64a) to one input of the monitor-error detector 64. A fourth control output of the control device 62a, at which a BUS (busy) signal appears is connected to an additional input of the status register 62 while a fifth control output of the verification device 62a at which an ITR (interrupt) signal appears is connected via a conductor 62b and via a second output of the interface circuit 21 to an "IRQ inverted" interrupt input of the microcomputer 50 (see FIG. 7).

Detailed Description Text (42):
A 3-bit address stored in the address register 52 (see FIG. 7) reaches the registers 58 to 62 via the address bus 56 (see FIG. 8) and selects one of the four first registers 58 to 61 for the storage of the following 8-bit data which come

h e b b g e e e f c e e e ge

from port C and also reaches via the bus connection 55, the drivers 53b and the data bus 57 (see FIG. 7) the registers 58 to 62 where they are stored in the register 58, 59, 60 or 61 selected by the address. These 8-bit data can be function module addresses and are in that case stored in form of a address byte in the address register 58. However they can also be a function indication destined for the function module 11, and in that case they are stored in form of a function byte in the function register 59. The actual data comprise preferably of two data bytes, i.e. one first data byte of greater magnitude and a second data byte of a lower magnitude. During a so-called writing cycle these two data bytes are transmitted from the control module 10 to the function modules 11 and are first stored for that purpose in the data register 60 or 61. The sequence in which these four bytes are loaded into the different registers 58 to 61 is optional, with the exception of the address byte which must always be loaded last. Immediately following the loading of the address byte into the register 58, the contents of all four registers 58 to 61 are loaded in parallel via the bus linkage 68 in form of a 32-bitword into the shift register 63. The loading of the address byte into the address register 58 thus starts a telegram transmission on condition that at least 25 microseconds have passed since the end of the last transmitted telegram. This is indicated by a logic value "1" of the BUS signal which is produced within the verification device 62a and appears at the latter's fourth control output. If this is not the case, the interface circuit 21 waits with the start of the telegram until the BUS signal assumes a logic value of "1". If all the starting conditions are met the bytes stored in the shift register 63 are then pushed out of said shift register 63 sequentially via the serial output and are carried via transmission unit 66 and bus 22 to the level adaptation circuit 20. The shift register thus operates here as a parallel/series converter. During a so-called writing cycle the address byte, the function byte, the data byte of greater magnitude and the data byte of lower magnitude are pushed in the sequence indicated out of the shift register 63 and are transmitted in form of four first bytes of a binary data telegram which has a total of 5 bytes to the function module 11. The fifth byte of this telegram on the other hand is transmitted in opposite direction in form of a so-called CRC byte following the reception of the fourth byte by the addressed function module 11 from the latter to the control module 10. During a so-called reading cycle only the address byte and the function byte are pushed out of the shift register 63 in the sequence indicated and are transmitted in form of two first bytes of a telegram which again has 5 bytes to the function modules 11. The data byte of greater magnitude, the data byte of lower magnitude and the CRC byte are then transmitted in the sequence indicated, following receipt of the second byte, in form of the last three bytes of the telegram in opposite direction from the addressed function module 11 to the control module 10.

Detailed Description Text (43):
The byte of the telegram received by the control module 10, i.e. the CRC byte during a writing cycle and the two data bytes as well as the CRC byte during a reading cycle sequentially reach an input of the monitor-error detector 64 via the level adaptation circuit 20, the bus 22 and the conductor 33 as well as an input of the multiplexer 65a and the serial input of the shift register 63 via the AND gate 67. The two data bytes received in the course of a reading cycle are pushed in sequentially into the shift register 63 from which they are then loaded in parallel into the corresponding registers 60 and 61 via the bus linkages 68. The shift register 63 thus functions here as a series/parallel converter. Since the function modules 11 do not transmit any address and function bytes, no received bytes are stored in the registers 58, 59. In FIG. 8 it was assumed for reasons of drawing simplification that the parallel outputs and the parallel inputs of the shift register 63 are identical.

Detailed Description Text (44):
The status of the control module 10 is stored in the status register 62. During the telegram transmission monitoring and CRC error checking tasks are carried out continuously. An error in telegram transmission detected during these two error

detections produces a logic value "1" at the output of the monitor-error detector 64 or of the OR gate 65c at the latest at the end of the telegram. The status of these two outputs is stored in readable form in two of the bits of the status register 62 which could be four in number for example, since the output of the monitor-error detector 64 and of the OR gate 65c are each connected to an input of the status register. The control module 10 is as a rule equipped with a "watch-dog" circuit which is not shown in the drawing of the control module 10. The fact that the watch-dog circuit had to intervene is indicated in an electrically readable manner by a logic value "1" in a third bit of the four bits of the status register 62. The process control within the interface circuit 21 is carried out by the verification device 62a. The status of the verification device 62a can be read off in form of a logic value "1" of the BUS signal in the fourth of the four bits of the status register. The verification device 62a furthermore reports to the microcomputer 50 at the end of each telegram by means of an interrupt ITR signal.

Detailed Description Text (46):
The time/serial output signal of the shift register 63 is synchronized by means of the clock signal CLK and the flipflop 66c and is then inverted and carried to the NAND gate 66d which is released if a writing cycle applies during the first four bytes of the telegram and if a reading cycle applies during the first two bytes of the telegram by means of the ES signal which is also produced in the verification device 62a. The monitor-error detector 64 only evaluates the bytes emitted from the control module 10. Each of these bytes emitted by the transmission unit 66 goes to an input of the monitor-error detector 64 over two different paths, i.e. on the one hand within the interface circuit 21 coming directly from the output of the transmission unit 66d and on the other hand (see FIG. 5) via the conductor 31 of bus 22, one of the two transmission circuits 23 of the level adaptation circuit 20, the reception circuit 24 and the conductor 33. The control module 10 thus monitors its own transmission and compares the transmitted data which reach the monitor-error detector 64 over different paths by means of the latter in order to give an alarm in case of non-agreement for the purpose of interrupting the telegram immediately and to cause its transmission to be repeated. The structure of the monitor-error detector 64 is shown in FIG. 20 and its manner of operation shall be explained later in the description of FIG. 20.

Detailed Description Text (47):
The AND gate 67 is released by means of the ER signal which is also produced in the verification device 62a, during the reception of the last byte if a writing cycle applies and during the reception of the last three bytes of the telegram if a reading cycle applies.

Detailed Description Text (49):
The interface circuit 25 of the function module 11 shown in FIG. 9 comprises a shift register 69, a bus multiplexer 70, an address comparator 71, an address encoder 72, a function decoder 73 in case that a received function byte is to be evaluated, an output stage 74 which comprises a buffer memory 75 and an output register 76 connected downstream by means of a bus 75a, a random code generator 77, an information encoder module 78, an optional input filter 79, a CRC generator 80 in case that a CRC byte is to be transmitted, a multiplexer 81, a monitor-error detector 82, a control device 83 and an output release gate 84. The interface circuit 25 is connected to the output circuit 44 of its function module 11 via an input bus 85 and an output bus 86. Within the interface circuit 25 the input bus 85 is connected in the indicated sequence either directly or via the input filter 79, a bus 79a, the bus multiplexer 70 and a bus 70a to a parallel input of the shift register 69. Two outputs of the module information encoder 78 are each connected over one pole via a control connection 87 or 88 to a control input of the output circuit 44. The output of the random code generator 77 is connected via a bus 77a, the output of the module information encoder 78 via a bus 78a, that of the input filter 79, if present, via bus 79a and that of the CRC generator 80 via a bus 80a, each to a bus input of the bus multiplexer 70 the output of which is connected in

turn via bus 70a to a first parallel input of the shift register 69. A bus 69a connects a parallel output of the shift register 69 to a bus input of the address comparator 71, a bus input of the function decoder 73 and to a bus input of the output stage 74. Within the output stage 74, bus 69a is connected to a data bus input of the buffer memory 75 whose data output is connected via bus 75a to a data bus input of the output register 76 whose data output in turn constitutes the data bus output of the output stage 74 which is again connected to the output bus 86. The address encoder 72 is connected via a bus 72a to a second bus input of the address comparator 71. The control device 83 is connected

Detailed Description Text (61):
The bus multiplexer 70 contains four groups of bus drivers, one of each is assigned respectively to the buses 77a of the random code generators 77, 78a of the module information encoder 78, 79a of the input filter 79 and 80a of CRC generator 80. Each group contains as many bus drivers as there are bus conductors provided for the corresponding buses 77a, 78a, 79a and 80a. Each bus driver is a "tri-state" driver and has a control input by means of which it can be switched on and off. The inputs of the bus drivers of one group are respectively connected within the bus multiplexer 70 to the bus conductors of the corresponding buses 77a, 78a, 79a or 80a while each of their outputs is connected to a bus conductor of the output bus 70a which is in common to all groups.

Detailed Description Text (63):
The transmission system works on the semi-duplex principle, i.e. the transmission alternates in both directions of transmission. At the same time a rigid master/slave principle is observed with utilization of a synchronized byte-oriented bit-serial transmission, whereby the information of a binary telegram is transmitted byte by byte in time. The control module 10 always supervises the bus connection as the master while each function module 11, as slave, is in turn supervised by the bus connection. The number of the transmitted bytes is constant per function module access and is preferably equal to 5 bytes of 8 bits each. The clock signal CLK supplied by the control module 10 and appearing on the synchronization conductor 30 serves synchronization as well as the control of reception on the function module side. Each function module 11 has a modular address which can be set on its address decoder 72 on the hardware and which can have 8 bits for example, so that 256 different modules are available for selection.

Detailed Description Text (64):
Every information addressed by a module address and, if present, by a channel number is called a data point. The information transmitted on the data conductor 32 comprises, as mentioned before, of 5 bytes of a binary telegram appearing in the following sequence on the bus connection 12; 14 at every function module access: address byte as the first byte, function byte as the second byte, first data byte as the third byte, second data byte as the fourth byte and CRC byte as the fifth byte.

Detailed Description Text (65):
During a writing cycle, i.e. when the direction of transmission of the two data bytes is from the control module 10 to the function module 11, the first four bytes are transmitted into the direction indicated while the fifth byte on the other hand, i.e. the CRC byte, is transmitted in opposite direction as an answerback communication from the function module 11 to the control module 10. During a reading cycle, i.e. when the direction of transmission of the two data bytes is from the function module 11 to the control module 10, the first two bytes are again transmitted in the direction going from the control module 10 to the function module 11 in order to call up a function module 11, but the last three bytes are transmitted in the opposite direction from the function module 11 to the control module 10. The first two bytes, i.e. the address byte and the function byte, are thus always transmitted in all cycles from the control module 10 to the function

module 11 and the fifth byte, i.e. the CRC byte is always transmitted from the function module 11 to the control module 10. The direction of transmission of the third and fourth bytes, i.e. of the two data bytes, depends however on the type of cycle. The two data bytes are thus produced either during a writing cycle in the control module 10 or during a reading cycle in a function module 11. Within each telegram, i.e. within each cycle, the direction of transmission of the two data bytes is however maintained and does not change. In each byte the MSB (most significant bit) is transmitted first as bit "7" and the LBS (least significant bit) is transmitted last as bit "0".

Detailed Description Text (66):
The clock signal CLK supplied by the control module 10 via the synchronization conductor 30 controls the applicable transmission cycle. All the function modules 11 constantly monitor on this conductor 30 and react immediately to any changes of the clock signal appearing therein. Each transmission cycle starts with a start condition on the synchronization conductor 30, contains a binary telegram and ends with a stop condition. A starting impulse carried by the control module 10 must appear for a minimum period of time ti on the synchronization conductor 30 so that the function module 11 can recognize the start as such. All the function modules 11 then actively switch themselves to the data conductor 32. The function modules 11 cannot become active by themselves on the bus connection 12; 14. A telegram can be interrupted by a new start at any time however.

Detailed Description Text (68):
Following the recognition of the start impulse the function modules 11 are ready to receive and evaluate the transmitted telegram and in particular its address byte. The data bites of the telegram are transmitted by the applicable transmitter over the data conductor 32 as the edge of the clock signal CLK drops and are scanned by the applicable receiver as the edge of the clock signal CLK rises.

Detailed Description Text (69):
If the synchronization conductor 30 remains for too long under a low voltage during a telegram, i.e. if the time period ti of an impulse gap of the clock signal CLK is greater than or equal to ti during a telegram, the function module 11 recognizes this as an error. The telegram is then interrupted and followed by a new start of the telegram with the next rising edge of the clock signal CLK. The function modules 11 react only at the end of a transmission cycle to any other errors.

Detailed Description Text (70):
The arrival of 5 bytes of 8 bits each, i.e. the arrival of the fortieth clock impulse after the recognition of the starting condition signals the end of the telegram to the function modules 11. Following this they still await a confirmation signal which must be sent by the control module 10 after the end of the telegram. If the control module finds, at the end of the telegram, that said telegram has been transmitted correctly it emits a confirmation signal "OK", comprising in that the duration t2 of an impulse of the clock signal is smaller than t.sub.o and that the duration t1 of the corresponding impulse gap is greater than or equal to ti, with t.sub.o having a value of 128 .mu.s, for example. However, if the control module finds at the end of the telegram that said telegram was not transmitted correctly it emits a confirmation signal "Not OK" comprising in that the duration t2 of an impulse of the tact signal CLK is greater than or equal to t.sub.o or in that the duration t1 of an impulse gap of the clock signal CLK is smaller than ti.

Detailed Description Text (71):
If the synchronization conductor 30 remains at a high voltage for too long a period during a telegram, i.e. if the duration t2 of an impulse of the clock signal CLK during a telegram is greater than or equal to t.sub.o, the function modules 11 cause a telegram interruption to occur, with subsequent expectation of a new start.

Detailed Description Text (72):
Each function module 11 which has received its own address must be provided with an error-free telegram within a period of time tw or a "watch dog" alarm is released in the corresponding function module 11. The period tw can be equal to 4 seconds, for example.

Detailed Description Text (73):
The frequency of the clock signal CLK is preferably 30 kHz to 80 kHz. Hereinafter it is assumed that this frequency has a value of 62.5 kHz. This is at the same time the bit frequency of the transmission telegram. A higher impulse number of the telegram is considered by the corresponding function module 11 to be a transmission error and the corresponding telegram is ignored.

Detailed Description Text (74):
The shift register 69 functions as a series/parallel or as a parallel/series converter. Upon reception of the starting impulse the address byte is pushed sequentially as the first one of the bytes received via conductor 35 into the shift register 69 of the interface circuit 25 of all the function modules 11 and, as soon as it is stored therein, is transmitted via bus 69a to the address comparator 71 in which the address received is compared with the modular address delivered by the address encoder 72 via bus 72a which is set by the hardware in the address encoder 72. If the two addresses do not agree, the function modules 11 concerned are locked to the reception of the following bytes of the telegram and they wait for a next start impulse while these bytes are pushed in time one after the other via conductor 35 sequentially into the shift register 69 of the non-locked function module 11, hereinafter the addressed function module 11 for short. The bits which are simultaneously pushed out at the serial output of the shift register 69 are prevented by the locked output release gate 84 from reaching the conductor 36.

Detailed Description Text (75):
The function byte which is then received by the addressed function module 11 as a second byte emitted by the control module 10 is pushed into the addressed function module 11's shift register 69 and is then loaded via bus 69a into the corresponding function decoder 73 for evaluation. The decoding of the function byte taking place in the function decoder 73 informs th addressed function module 11 in detail on the type of the information still to be transmitted in the third and/or fourth byte of the current telegram.

Detailed Description Text (76):
The LSB of the function byte determines for example the direction of transmission of the third and fourth byte. If this LSB has a logic value of "1", this means for example that the control module 10 wishes a reading cycle and expects information from the addressed function module 11 in the transmitted third and/or fourth byte of the telegram. If this LSB has a logic value of "0" however, this means that the control module 10 wants a writing cycle and will itself transmit information to the addressed function module 11 in the third and/or fourth byte of the telegram.

Detailed Description Text (77):
Theoretically an additional 2.sup.7 =127 different function data are possible as contents of the 8 bits of the function byte per address for the direction of transmission. In order for the function module 11 not to switch over to another function in case of a bit error in the data conductor 32, a great Hamming distance is selected between two function byte values used as code words so that in addition to the direction of transmission of the data bytes, the function byte now only contains four function data, i.e. so that the addressed function module 11 must send either a so-called "address polling telegram", a module information telegram or an actual data telegram as the third and/or fourth byte during a reading cycle. In a writing cycle on the other hand, only one actual data telegram is transmitted as the third and fourth bytes. For function modules 11 with analog input/output, a function module 11 contains as a rule several data channels. In that case, be it

during a reading or a writing cycle, a bit of the function byte indicates during the transmission of an actual data telegram which of the data channels of the addressed function module 11 is to be described or read.

Detailed Description Text (78):
The so-called "address polling" represents a control over multiple use of a particular module address. Each function module 11 which is put into action by the transmitted address sets one single and randomly selected bit in the third of fourth byte to a logic value of "1". In this way only one logic value "1" exists in teh total of 16 bits of the third and fourth byte during an address polling cycle and can appear at any location in one of the two bytes and is produced by the random code generator 77. Shortly before the transmission of the third and fourth byte by an addressed function module 11 their contents are loaded in parallel by the random code generator 77 starting via bus 77a, then bus multiplexer 70 and bus 70a into the shift register 69 and are thereupon carried sequentially via the serial output of said shift register 69 and via the output release gate 84 which is released during a reading cycle as the third and fourth byte to the conductor 36 and thereby also to the conductor 32. If several function modules 11 can erroneously be reached at one and the same module address, the control module 10 recognizes this because several logic values "1" are contained in the third and/or fourth byte of the received telegram instead of only one single logic value "1".

Detailed Description Text (79):
A module information telegram on the other hand contains information on the addressed function module 11 which are set at the hardware level in the module information encoder 78 and are loaded in parallel into the shift register 69 shortly before the transmission of the third and fourth byte via bus 78a, bus multiplexer 70 and bus 78a to be then transmitted sequentially to the conductors 36 and 32, similarly as the address polling telegram. In the third byte an information concerning the structure and/or the input and output configuration of the pin occupation of the addressed function module 11 for example is given, while an information on the type of an integrated LSI (large scale integrated) circuit printed in the addressed function module 11 is given in the fourth bit.

Detailed Description Text (80):
The bits of an actual data telegram which is to be transmitted as third and fourth byte during a read cycle from the function module 11 to the control module 10 reach the interface circuit 25 of the addressed function module 11 coming from the output circuit 44 and going via the input bus 85 and the input filter 79 where they are stored temporarily bit by bit to be loaded in parallel later, shortly before transmission, via bus 79a, bus multiplexer 70 and bus 70a into the shift register 69 from which they are transmitted sequentially to the conductors 36 and 32, similar to the address polling telegram and the module information telegram.

Detailed Description Text (81):
If the control module 10 informs the function module 11 by means of the function byte on the other hand that a writing cycle applies, this function module 11 awaits the third and fourth bytes of the telegram which are transmitted by the control module 10 and pushes them upon receipt via conductor 35 sequentially into the shift register 69 from which they are loaded in parallel and byte by byte first into the buffer memory 75 and then into the output register 76, to be then transmitted via the output bus 86 to the output circuit 44.

Detailed Description Text (82):
The control device 83 shown in FIG. 10 comprises a clock generator 102, a first control unit 103, a second control unit 104, a frequency divider 105, a watch-dog counter 106 an AND gate 107 and two invertors 108 and 109. The clock generator 102 produces a preferably rectangular clock signal with a frequency of 4 MHz, for instance, and which shall be called the 4-MHz clock signal hereinafter. This 4-MHz clock signal is transmitted via a cable connection to a clock input of each of the

components 103, 104, 105 and 106 as well as to a first conductor of each of the control busses 90, 91, 92, 94, 95, 96 and 98. The clock signal CLK coming from the control module 10 reaches via conductor 34 a second clock input of the first control unit 103 which is provided with six outputs at each of which a signal T1, T2, T3, STRT (START), ACK (ACKNOWLEDGE) and C127 appears. Each of these six outputs of the control unit 103 is carried to a control input of the second control unit 104. The frequency divider 105 has the control bus 93 as an output bus as well as an additional two single-pole outputs at which a 1-MHz clock signal or a 64-Hz clock signal appears. The 1-MHz clock signal is carried via a conductor to a third clock input of the control unit 103 while the 64-Hz clock signal supplies a first input of the watch-dog counter 106 as well as a second conductor of the control bus 94. The ACK signal coming from the control unit 103 reaches a second input of the watch-dog counter 106 whose output, at which a WDR signal appears, is linked with an additional input of the control unit 104 and a second conductor of the control bus 98. The control bus 89 is also carried to a bus connection of the control unit 104 which has eight single-pole outputs at each of which a signal B40, ACLD, ARLD, B23, MILD, OUT, OULLD and OURLD appears. The output with the B40 signal is connected to an additional input of the control unit 103 while the outputs with the ACLD, SRLD, B23 and MILD signals are each connected to a second conductor of the control bus 90 or 91 or 92 or 95. The output with the OUT signal is carried to the cable connection 101 while the outputs with the OULLD and OURLD signals are connected to the third or fourth conductor of the control bus 98. The conductor on which the MR signal occurs is connected to an additional input of the control unit 104. The control bus 90 has four conductors. A signal AMN occurs at the third of these conductors and is carried to a last input of the control unit 104 while the STRT signal coming from the control unit 103 supplies the fourth conductor of the control bus. The control bus 91 has three conductors of which the third is supplied with the signal T3 coming from the control unit 103. The control bus 92 has three conductors of which the third is supplied by the STRT signal which is also carried to the input of the invertor 109 whose output supplies a third conductor of the control bus 95 or a second conductor of the control bus 96 with a STRTN signal. An MF signal occurs on the input conductor 99 of the control device 83 and is carried to a last input of the control unit 103 as well as to an input of the invertor 108. The output of the invertor 108 is connected to a first input of the AND gate 107 whose output, at which a CRE signal occurs, is carried to a third conductor of the control bus 96. The T2 signal comes from the control unit 103 and supplies a second input of the AND gate.

Detailed Description Text (84):
The watchdog counter 106 can comprise for instance of a synchronous 9-bit counter which can be reset to zero and which counts the periodic rectangular impulses of the 64-Hz clock signal. When 2.sup.9 impulses of the 64-Hz clock signal reach the input of the watchdog counter 106, i.e. after a period of 4 seconds, without the watchdog counter 106 having first been reset to zero by the ACK signal, a logic value "1" appears at the Q output of the eighth bit of the watchdog counter 106 for a period of 250 ns, representing a WDR signal which simultaneously resets the watchdog counter 106 to zero via a feedback at the reset input of said watchdog counter 106. The logic value "1" of the WDR signal indicates that no valid telegram confirmed by an ACK signal has reached the corresponding function module 11. The watchdog counter 106 is set back to zero by every ACK signal and then again begins to count.

Detailed Description Text (86):
The input of the control unit 103 at which the 4 MHz clock signal appears is carried to the clock input of the synchronizer 114, of the delay link 115, of the clock signal-status memory 116 and of the counter 117 as well as of the flipflops 127, 131 and 132. The input of the control unit 103 at which the clock signal CLK occurs is connected to a second clock input of the synchronizer 114 and to one of the clock signal-status memory 116. A first output of the synchronizer 114 at which an EDG (edge) signal appears is carried to an additional input of the clock signal-

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status memory 116 and to one of the counter 117 while its second output is connected to an input of the delay link 115 which has three outputs constituting three outputs of the control unit 103 at each of which a signal T1, T2 or T3 appears. An output of the clock signal-status memory 116 is carried to a first input of the AND gate 119 as well as via invertor 120a to a first input of the AND gate 120. The parallel output of the counter 117 is connected via a bus input of the decoder 118, the first output of which is carried to a second input of the AND gate 120. The output of the AND gate 119 at which a signal C22 appears is connected to a first input of the NOR gate 121, to one of the AND gate 125 and to one of the AND gate 130 while the output of the AND gate 120 at which the signal C127 appears is carried to a second input of NOR gate 121 as well as to an output of the control unit 103. The output of the NOR gate 121 is connected to a first input of the AND gate 122, the second input of which is carried to the input of the control unit 103 at which the 1-MHz clock signal appears and the output of which is connected to a release input of the counter 117. The output of the delay link 115 at which the T3 signal appears is carried via invertor 123 to a first input of the AND gate 124, the output of which is connected to a first input of the OR gate 126. The output of the delay link 115 at which the T1 signal appears is carried to a second input of the AND gate 125, the output of which is connected to a second input of the OR gate 126, whereby its output is in turn carried to the D input of the flipflop 127. A STRT signal which is carried to a second input of the AND gate 124, to a first input of the OR gate 129 and to an output of the control unit 103 appears at the Q output of the flipflop 127. The two inputs of the control unit 103 at which the signals MF and B40 appear are connected to a first input of the NOR gate 128 or to a second input of the AND gate 130. The output of the NOR gate 128 supplies a second input of the OR gate 129 and a third input of the AND gate 130. The output of the OR gate 129 is carried to the D-input of the flipflop 131, the inverted Q-output of which is connected to a second input of the NOR gate 128. The output of the AND gate 130 is carried to the D-input of the flipflop 132, the Q-output of which is connected to a third input of the NOR gate 128 and constitutes at the same time the output of the control unit 103 at which the ACK signal appears.

Detailed Description Text (88):
Each transmitted telegram starts with a start impulse in the CLK clock signal the duration of which, also called "idle time", is at least 22 .mu.s. The starting impulse is an impulse gap in the control module and is an impulse in the function module 11 because of its inversion in the transmission circuit 23 of the control module 10 (see FIG. 5). If an impulse of the CLK clock signal has a duration of at least 22 .mu.s at the input of the time counter 111, the counter 117 counts at least 22 periods of 1 .mu.s each of the 1-MHz clock signal and reaches at least the counted value 22 which represents a start signal for the reception of a telegram to the function module 11. For that purpose the decoded counted value 22 of the counter 117 releases the AND gate 119 so that a logic value "1" on the one hand appears as a C22 signal at an output of the time counter 111 and thereby appears at one input each of the AND gates 125 and 130 and is locked on the other hand via the NOR gate 121 and the AND gate 122 so that no 1-MHz clock impulse can reach the counter 117 any longer and so that the latter stops at the counted value 22 until it is again reset by the EDG signal when the next edge of the CLK clock signal appears which, as an impulse-end edge, is a trailing edge. At that moment an impulse of the T1 signal also appears coming from an output of the delay link 115 at an input of the AND gate 125 of the start detector 112, so that the C22 signal reaches the flipflop 127 in which its logic value "1" is stored by the 4 MHz clock signal via the OR gate 126, whereby the flipflop 127 is kept via the AND gate 124 and via the OR gate 126 in that logic state until 500 ns later the T3 signal coming from the delay link 115 via the invertor 123 briefly locks the AND gate so that the 4 MHz clock signal loads a logic value "0" into the flipflop 127 and thereby resets the latter back to zero. At the output of the flipflop 127 and thereby of the start detector 112 a continuous impulse lasting 500 ns thus appears as a STRT signal starting the reception of the telegram in the function module 11 when a start

impulse is present in the CLK clock impulse. Every telegram transmitted ends with stop impulse in the CLK clock signal the duration of which, also called "timeout" period, is 127 .mu.s. The stop impulse is an impulse in the control module 10 and, because of its inversion in the transmission circuit 23 of the control module (see FIG. 5), an impulse gap in the function module 11. If an impulse gap of the clock signal CLK at the input of a time counter 111 has a duration of at least 127 .mu.s, the counter 117 counts at least 127 periods of 1 .mu.s each of the 1-MHz clock signals and reaches at least the counted value 127. The decoded counted value 127 of the counter 117 releases the AND gate so that a logic value "1" appears on the one hand in form of a C127 signal at an output of the time counter 111 and so that the AND gate 122 is locked via the NOR gate 121 on the other hand so that no 1-MHz clock impulses any longer reach the counter 117 and so that the latter stops at the counted value 127 until it is again reset by the EDG signal when the next edge of the CLK clock signal appears.

Detailed Description Text (89):
Following the start impulse and before the stop impulse the counter 117 does not normally reach the counted value 22 or 127, so that no logic value "1" appears at the outputs of the time counter 111 in that case. If the impulse of the CLK clock signal at the input of the time counter 111 lasts too long for any reason, a start impulse is simulated. The telegram is interrupted immediately and a new start of the telegram is initiated.

Detailed Description Text (90):
When the STRT signal assumes the logic value "1" at the fulfillment of the start conditions, the flipflop 131 of the acknowledgment generator 113 is set via the OR gate 129 and thereby the AND gate 130 is released via the NOR gate 128. This means that the corresponding function module 11 expects to receive an acknowledgment signal. When a monitoring error has been detected by the monitor-error detector 82 of the interface circuit 25 (see FIG. 9), a logic value "1" appears as an MF signal coming from the monitor-error detector 82 and going via the cable connection 99 at an input of the control device 83 and of the control unit 103. If a monitoring error exists the MF signal resets the flipflop 131 via the NOR gate 128 and the OR gate 129 and no acknowledgment signal of a correct telegram transmission is issued until a new telegram start takes place. If no monitoring error exists, the flipflop 132 is set at the end of the telegram by means of the B40 signal via the AND gate 130 if the C22 signal has a logic value "1", i.e. if the impulse gap at the end of the telegram has at least the length of a start impulse. AT the Q output of the flipflop 132 a logic value "1" then appears as an ACK acknowledgement signal of a correct telegram transmission. The ACK acknowledgment signal also supplies an input of the AND gate 140 of the control unit 104 (see FIG. 12).

Detailed Description Text (92):
The control unit 104 is supplied via the control bus 89 with five signals, FWR, FAP, FMI, RWN and FELS. Furthermore there are ten input signals, i.e. the 4 MHz clock signal and the signals T1, T2, T3, MR, AMN, STRT, ACK, C127 and WDR as well as, in addition to the output signals present in the control busses 89 and 97, another eight output signals, i.e. OURLD, OULLD, OUT, MILD, B23, SRLD, ACLD and B40, each of which appears at a single-pole output of the control unit 104. The 4 MHz clock signal supplies a sixth conductor of the control bus 89, a clock input of the counter 148 as well as the clock inputs of the flipflops 154 and 162. The ACK signal supplies a first input and the FWR signal a second input each of the AND gate 140 whose output constitutes the output of the control unit 104 at which the OURLD signal appears. The T1 signal supplies a first input of each of the AND gates 141, 134 and 163. The T2 signal supplies a first input of each of the AND gates 150, 159 and 138. The T3 signal supplies a first control input of the counter 148 whose parallel output is carried to a bus input of the decoder 149 which in turn has five outputs at each of which a signal B7, B15, B23, B31 and B40 appears, as well as a sixth output which is carried to a second control input of the counter 148 and to a first input of the NOR gate 151. The B31 signal supplies a second

input of the AND gate 141, a first conductor of the control bus 97, a first input of each of the OR gates 160 and 139 as well as via invertor 142 a first input of each of the NAND gates 145, 143 and 144. The output of the AND gate 141 constitutes the output of the control unit 104 at which the OULLD signal appears. The FAP and FMI signals each supply a second input of the NAND gate 143 or 144. The output of the NAND gate 143 is carried to a second input of the NAND gate 145 and via invertor 147 to a second conductor of the control bus 97. The output of the NAND gate 144 is connected to a third input of the NAND gate 145 and, via invertor 146, to a third conductor of the control bus 97. The output of the NAND gate 145 in turn supplies a fourth conductor of the control bus 97. The B15 signal supplies on the one hand a second input of each of the AND gates 134 and 150 as well as of the OR gate 139 and on the other hand a first input of the AND gate 139. The output of the AND gate 134 at which an FDLD signal appears, is carried to a seventh conductor of the control bus 89. The FELS signal supplies a third input of the AND gate 150 the output of which is carried to a second input of the NOR gate 151. Each of the signals AMN, C127 and WDR supplies an additional input of the NOR gate 151, the output of which is connected to a first input of the AND gate 152. The output of the AND gate 152 is carried to a first input of the NOR gate 153, the output of which is connected to the D input of the flipflop 154. The STRT signal supplies a second input of the NOR gate 153 and a first input each of the NOR gates 156 and of the OR gate 155, while the MR signal supplies an inverting reset input of the flipflop 154. The inverting Q output of the flipflop 154 is carried to a second input of the AND gate 152 and its Q output to a second input each of the OR gate 155 and of the NOR gate 156. The B40 signal supplies a third input of the NOR gate 156 and an output of the control unit 104. The output of the NOR gate 156 is connected to a first input of the AND gate 157, the output of which is carried to a first input of the OR gate 161. The output of the OR gate 161 is connected to the D input of the flipflop 162 while its Q output, at which the OUT signal appears, is carried to a second input each of the AND gates 157 and 163 as well as to the cable connection 101 of the output of the control unit 104. At the output of the AND gate 163 the MILD signal appears and supplies an additional output of the control unit 104. The RWN signal supplies a second input of the AND gate 158, the output of which is connected to a second input of the OR gate 160. The output of the OR gate 160 is carried to a second input of the AND gate 159, the output of which is in turn connected to a second input of the OR gate 161. The B23 signal supplies a third input of the OR gate 139 and an additional output of the control unit 104 while the output of the OR gate 139, at which the SRLD signal appears, constitutes another output of the control unit 104. The B7 signal supplies a second input of the AND gate 138 the output of which, at which the ACLD signal appears, constitutes a last output of the control unit 104. The output of the OR gate 155 is connected to a third control input of the counter 148.

Detailed Description Text (93):
The counter 148 of the bit counter 135 can be a synchronous 6-bit counter the counted value of which is decoded continuously in the downstream decoder 149. Since the bit frequency of the telegram and the frequency of the CLK clock signal are of equal magnitude and have a value of nearly 62.5 kHz and since the frequency of the T3 signal, the impulses of which are counted by the counter 148, is equal to this bit frequency, the counter 148 counts the number of bits of the telegram. For that purpose the STRT output signal of the start detector 112 which goes to the counter 148 via the OR gate 155 resets the counter 148 to zero upon recognizing the starting conditions, and the latter then counts the impulses of the T3 signal and thereby the bit impulses. The decoder 149 decodes the counted values 7, 15, 23, 31, 40 and greater than 40. The output signals B7, B15, B23, B31 and B40 accordingly take on the logic value "1" after the 9th, 16th, 24th, 32nd and 41st telegram bit, i.e. at the end of each byte, and this indicates the presence of the corresponding byte end. At the same time the decoder 149 is also provided with an overflow output at which a logic value "1" appears if more than 41 impulses of the T3 signal are counted by the counter 148. This logic value "1" is carried to an input of the counter 148 and stops the counting process within same by denying access to the

first step of the counter 148 by means of an AND gate. Simultaneously logic value "1" also reaches an input of the NOR gate 151 of the NOP reset circuit 136. The counting process of the counter 148 remains interrupted until a new impulse of the STRT signal again sets the counter 148 back to zero.

Detailed Description Text (98):
4. More than 40 telegram bits have been transmitted, i.e. the overflow output signal of the decoder 149 has a logic value "1".

Detailed Description Text (101):
Upon initiation of a general reset (master reset) the flipflop 154 is set at a logic value "1". When a starting condition has been met the STRT signal resets the flipflop 154 to zero via the NOR gate 153. When one of the first five above-mentioned events occurs, a logic value "0" appears at the output of the NOR gate 151 and locks the AND gate 152 so that a logic value "1" appears at the D input of the flipflop 154 and is then loaded into the latter by the 4 MHz clock signal. A logic value "1" appears at the output of the transmission release circuit 137 when the addressed function module 11 is to transmit. The flipflop 162 is always set at the end of a telegram because the last byte of a telegram, i.e. the CRC byte, is always provided by the function module. The flipflop 162 which has a latch in form of the AND gate 157 and the OR gate 161, is reset to zero by the STRT signal, by the B40 signal corresponding to a 41st T3 impulse or by the output signal of the NOP reset circuit 136 via the NOR gate 156. The flipflop 162 is set on the one hand after receipt of a second byte, i.e. when the B15 signal has a logic value "1" when the decoded function is a read function, i.e. when the RWN signal coming from the function decoder 73 reaches the control device 83 and the control unit 104 via control bus 89. In other words, when a logic value "1" appears at the output of the AND gate 158 the flipflop 162 is set by the 4 MHz clock signal. On the other hand the flipflop 162 is also set via the OR gate 160 each time the fifth byte of the telegram must be sent, i.e. when the B31 signal has a logic value "1". This occurs only when the T2 signal has a logic value "1" since it is only then that the AND gate 159 is released The OUT signal at the Q output of the flipflop 162 releases via cable connection 101 the output release gate 84 of the interface circuit 25 (see FIG. 9) and the AND gate 217 in the multiplexer 81 (see FIG. 19), causing among other things the serial output bits of the shift register 69 to reach the conductor 36 (see FIG. 9). At the same time the OUT signal reaches the monitor-error detector 82 (see FIG. 9) in form of a MILD signal via the AND gate 163 (see FIG. 12) and via the control bus 95 (see FIG. 10) when the T1 signal has a logic value "1".

Detailed Description Text (104):
When the signals B7 and T2 assume a logic value "1" at the end of a first byte a logic value "1" as the ACLD signal (address comparator: load) appears via the AND gate 138 (see FIG. 12) and the control bus 90 (see FIG. 10) at one input of the AND gate 167 of the address comparator 71 (see FIG. 13) and releases it. The address received as first byte appears via bus 69a at the first inputs of the comparison circuits 170 while the module address of the function module 11 which is set in hardware appears via bus 72a at the second inputs of the comparison circuit 170. If two identically numbered bits of the two addresses are different, the output of the AND gate 169 has a logic value "0". The latter is inverted in the NOR gate 165 and the inverted value is then stored in the flipflop 164 by means of the 4 MHz clock signal to appear as an AMN signal at an output bus conductor of the control bus 90. The AND gate 166 is used as a locking circuit of the flipflop 164 for the case that both addresses should be identical, so that a logic value "0" must be stored in the flipflop 164. The ACLD signal cancels this locking function by locking the AND gate 166 via invertor 168. At the same time the output signal of the AND gate 169 is read by means of the AND gate 167.

Detailed Description Text (107):
If the signals B15 and T1 assume a logic value `1` at the end of the second byte in

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an addressed function module 11, a logic value "1" appears as a FDLD (function decoder: load) signal via the AND gate 134 (see FIG. 12) and the control bus 89 (see FIGS. 10 and 9) at an input of the memory circuit 171 of the function decoder 73 (see FIG. 14). The bits of the second telegram byte, which are thus given a meaning, are stored at that moment in the flipflop 176 of the memory storage 171 by means of the 4 MHz clock signal following the cancellation, by the FDLD signal and via invertor 172, of the locking of the flipflop 176 which has in the meantime been locked by the AND gate 174. The second telegram byte stored in the memory circuit 171 is decoded by means of the decoder 177 and a logic value "1" appears as a signal FAP, FMI, FWR or RWN at an output of the function decoder 73 when the second telegram byte indicates an "address polling" function, module information, write cycle or data direction. If the second byte does not contain any valid function indication, a logic value "1" appears at the output of the NOR gate 178 as a FELS signal, and thereby at an additional output of the function decoder 73. The signals FAP, FMI, FWR, RWN and FELS reach the control device 83 (see FIG. 9) and the control unit 104 (see FIG. 10) via the control bus 89.

Detailed Description Text (108):
In the control unit 104 (see FIG. 12) the FAP signal, whose logic value "1" demands an "address polling" telegram as the third and fourth byte, goes via the normally released NAND gate 143, via the invertor 147 and the control bus 97 to an input of the bus multiplexer 70 (see FIG. 9) which is connected within the latter to all the control inputs of those bus drivers which are assigned to the bus 77a of the random code generator 77.

Detailed Description Text (109):
Within the control unit 104 (see FIG. 12) the FMI signal, whose logic value "1" demands a module information telegram as the third and fourth byte, goes via the normally released NAND gate 144, via the invertor 146 and the control bus 97 to an additional input of the bus multiplexer 70 (see FIG. 9) which is connected within the latter to all the control inputs of those bus drivers which are assigned to the bus 78a of the module information coder 78.

Detailed Description Text (110):
The two signals FAP and FMI go in inverted form via the normally released NAND gates 143 and 144 to the nand gate 145 (see FIG. 12). If both the FAP and the FMI signal have a logic value "0" neither an address polling nor a module information telegram is demanded as the third and fourth byte, and the third and fourth bytes in this case are always actual data bytes whose bits go in a read cycle via the input bus 85 and the input filter 79 to the bus multiplexer 70 (see FIG. 9). In this case a logic value "1" appears at the output of the NAND gate 145 and goes via the control bus 97 to an additional input of the bus multiplexer 70 (see FIG. 9) which is connected within the latter to all the control inputs of those bus drivers which are assigned to the bus 79a of the input filter 79.

Detailed Description Text (111):
In all three cases the NAND gates 143, 144 and 145 are locked at the end of the third byte by the B31 signal via invertor 142 since a that moment at the latest the contents of the fourth byte must already be loaded into the shift register via bus multiplexer 70. At the same time the logic value "1" of the B31 signal goes via the control bus 97 and reaches an additional input of the bus multiplexer 70 (see FIG. 9) which is connected within the latter to all the control inputs of those bus drivers which are assigned to the bus 80a of the CRC generator 80, thus preparing the loading process of the bits of the fifth telegram byte into the shift register 69.

Detailed Description Text (113):
The output register 76 contains one memory circuit 185 per bit of the data byte, each memory circuit 185 comprising a flipflop 186, a NOR gate 187 and two AND gates 188 and 189 as well as of an invertor 190. The memory circuits 171 (see FIG. 14)

and 179 are of identical structure while the memory circuits 179 and 185 are of nearly identical structure, with the only difference that the NOR gate 180 has only two inputs while the NOR gate 187 has three inputs. Four signals, the 4 MHz clock signal as well as the signals OULLD OURLD and WDR reach the output stage 74 via the four bus conductors of the control bus 98. The 4 MHz clock signal supplies the clock inputs of all the flipflops 184 and 186 of the memory circuits 179 or 185. The OULLD signal supplies an input of all the memory circuits 179 while the OURLD and WDR signals supply all the first or all the second inputs of the memory circuit 185. The input of each memory circuit 179 is connected within the latter to a first input of the AND gate 181 and, via invertor 183, to a first input of the AND gate 182. One bus conductor of bus 69a is connected to a second input of the AND gate 181 of the corresponding memory circuit 179 while the inverting Q output of the flipflop 184 constitutes the output of the corresponding memory circuit 179. Each of the outputs of all the memory circuits 179 is connected to a bus conductor of the bus 75a and via same to a first input of the AND gate 188 of the corresponding memory circuit 185. The first input of each memory circuit 185 is connected within same to a second input of the AND gate 188 and, via invertor 190, to a first input of the AND gate 189. The second input of each memory circuit 185 is connected within same to the third input of the NOR gate 187. Each of the inverted Q outputs of the flipflop 186 of all the memory circuits 185 is connected a bus conductor of the output bus 86.

Detailed Description Text (115):
If the ACK signal has a logic value "1" at the end of the fifth telegram byte, i.e. if a correct telegram has been transmitted and the function byte has declared a write cycle, i.e. if the FWR signal has a logic value "1", a logic value "1" appears at the output of the AND gate 140 (see FIG. 12) as an OURLD (output register:load) signal, which signal reaches an input of the output stage 74 and of the output register 76 via control bus 98 (see FIGS. 10 and 9) and which loads the bit values buffer-stored in the buffer memory 75 via bus 75a into the memory circuit 185 of the output register 76 when the WDR signal of the watchdog counter has a logic value "0". These bit value are then stored in the flipflops 186 of the memory circuits 185. The latter have locking mechanisms which are realized by means of the invertor 190 and of the AND gate 189. The bit values stored in the output register 76 are directed via output bus 86 to the output circuit 44 of the function module 11 where they undergo further processing. If a logic value "1" appears as a WDR signal at one of the inputs of the output stage 74 and of the output register 76, said output register 76 is reset to zero via the NOR gate 187. The WDR signal reaches output stage 74 from the output of the watchdog counter 106 (see FIG. 10) and via the control bus 98.

Detailed Description Text (116):
The random code generator 77 shown in FIG. 16 can be supplied via the bus conductors (e.g. four) of the control bus 93 with four random bits and via the three conductors of the control bus 92 with the 4-MHz clock signal and the signals STRT and B23. The random code generator 77 contains per bus conductor of the control bus 93 one memory circuit 191 comprising an invertor 192 and two AND gates 193 and 194, one NOR gate 195 and one flipflop 96. The memory circuit 191 is of identical structure as the memory circuits 171 and 179. The 4-MHz clock signal supplies the clock inputs of all the flipflops 196 while the STRT signal supplies one input of all the memory circuits 191. The input of each memory circuit 191 is carried within the latter to a first input of the AND gate 193 and via the invertor to a first input of the AND gate 194, while the inverted Q output of the flipflop 196 constitutes the output of the memory circuit 191. Each of the outputs of the memory circuits 191 of the three lowest bits is carried to a bus conductor of a bus 197. The random code generator 77 also contains an exclusive-OR gate 198 and a "3 to 8" decoder 199, the output of which constitutes the bus 77a which represents the output bus of the random code generator 77. The bus 197 constitutes the input bus of the "3 to 8" decoder while the output of the fourth memory circuit 191 in which the highest-value bit of the four random bits is stored is connected to a first

input of the exclusive-OR gate 198 whose second input is supplied by the B23 signal and whose output is carried to an additional input of the "3 to 8" decoder 199.

Detailed Description Text (117):
Two bytes, i.e. the third and fourth byte of the telegram, are produced in the random decoder 77, whereby the 16 bits of the two bytes contain only one single bit with the logic value "1" which furthermore is in a random position within one of the two bytes. The four random bits which are produced in the frequency divider 105 of the control device 83 (see FIG. 10) appear at the control bus 93 at the input of the memory circuit 191 of the random code generator 77 and, upon recognition of the start condition given by the logic value "1" of the STRT signal, are loaded into same where they are stored in the flipflop 196. Each of the memory circuits 191 has a locking circuit which is realized by means of the invertor 192 and the AND gate 194. The first three bits of the 4-bit random value thus stored are decoded in the "3 to 8" decoder 199. The byte (third or fourth), in which the logic value "1" should be found is selected by means of the fourth bit of the 4-bit random value. This is done through the exclusive-OR gate 198 the output of which releases the "3 to 8" decoder 199 when its output has a logic value "0", i.e. when its two input signals are identical. Since one of these input signals, i.e. the B23 signal, has a logic value "1" only at the end of the third telegram byte, the "3 to 8" decoder 199 is released only at the beginning of the fourth byte and the logic value "1" is transmitted only during the fourth byte, when the fourth bit of the 4-bit random value has a logic value "1". If on the other hand the fourth bit of the 4-bit random value has a logic value "0", the "3 to 8" decoder 199 is released already at the beginning of the third byte so that the logic value "1" is transmitted already during the third byte. In that case the "3 to 8" decoding is locked at the beginning of the fourth byte so that it may not provide any logic value "1". The "3 to 8" decoder 199 generates a logic value "1" at only one of its outputs, this output being determined by the 3-bit input value of the "3 to 8" decoder 199.

Detailed Description Text (119):
Each bus conductor of the input bus 85 is carried to a first input of the AND gate 202 of a first memory circuit 200 of its corresponding bit filter 79b. In each bit filter 79b, the output of the first memory circuit 200 is carried to a first input of the AND gate 202 of a second memory circuit 200, of the NAND gate 206 and of the NOR gate 207, while an output of the second memory circuit 200 is carried to a first input of the AND gate 202 of the third memory circuit 200 and to a second input of the NAND gate 206 and of the NOR gate 207. In each bit filter the output of the third memory circuit 200 is connected to a third input of the NAND gate 206 and of the NOR gate 207. In each bit filter 79b, the output of the NAND gate 206 is carried to a first input of the AND gate 208 whose second input is connected to the inverted Q output of the flipflop 210. Each of the outputs of the AND gate 208 and of the NOR gate 207 is carried to an input of the NOR gate 209 whose output is connected to the D input of the flipflop 210. The Q output of the flipflop 210 constitutes the output of the corresponding bit filter 79b. The outputs of all the bit filters 79b are carried to a bus conductor of the bus 79a which constitutes the output bus of the input filter 79. The input filter 79 is supplied via the two bus conductors of the control bus 94 with the 4-MHz clock signal and with the 64-Hz clock signal. The 4-MHz clock signal supplies the clock inputs of all the flipflops 205 and, via invertor 209a, the clock inputs of the flipflops 210. The 64-Hz clock signal supplies in all the bit filters 79b the input of all the memory circuits 200. This input is connected within each memory circuit to a second input of the AND gate 202 and, via invertor 201, to a first input of the AND gate 203.

Detailed Description Text (121):
The CRC generator 80 shown in FIG. 18 comprises a shift register 211 and three adders 212, 213 and 214. Each adder 212, 213, 214 functions as "Modulo 2 adder" and comprises an exclusive-OR gate. The CRC generator 80 generates a CRC byte which has preferably eight bits. In that case the shift register 211 also comprises eight bit cells 0 to 7. The 8-bit parallel output of the shift register 211 constitutes the

bus 80a which represents the output bus of the CRC generator. The cable connection 81a coming from the multiplexer 81 (see FIG. 19) is carried to a first input of the adder 212, the second input of which is connected to the output of the bit cell 7 of the shift register 211 and the output of which is connected to a first input each of the adder 213 and 214 as well as to a input of the bit cell 0 of the shift register 211. A parallel output of the bit cell 6 is carried to a second input of the adder 213, the output of which is connected to a parallel input of the bit cell 7. A parallel output of the bit cell 1 is carried to a second input of the adder 214, the output of which is connected to a parallel input of the bit cell 2. The 4-MHz clock signal as well as the signals STRTN and CRE are carried via three conductors of the control bus 96 to the CRC generator 80. The 4-MHz clock signal feeds the clock inputs of all the bit cells of the shift register 211. Each of the signals STRTN and CRE supplies an additional input of the shift register 211.

Detailed Description Text (123):
During the time in which telegram bytes are to be received through the function module 11, a logic value "0" appears on the cable connection 101a so that the AND gate 217 is locked and the AND gate 216 is released. The time-sequential bits of the telegram received in the conductor 35 thus reach the input of the CRC generator 80 via the AND gate 216 and the conductor 81a. If on the other hand bytes are to be sent by the function module 11, a logic value "1" appears on the cable connection 101 and releases the output-release gate 84 (see FIG. 9) on the one hand and on the other hand the AND gate 217 while the AND gate 216 is locked at the same time. The time-sequential bits of the transmitted telegram then go from the serial output of the shift register 69 via the AND gate 217 and the conductor 81a to reach the input of the CRC generator 80 (see FIGS. 9 and 19).

Detailed Description Text (124):
Thus the received and transmitted bits of the telegram are all pushed into the input 1a of the CRC generator 80 and thereby into its feedback shift register 211 in a time-sequential manner (see FIG. 18). The CRC generator generates the CRC byte (cyclic redundant check byte) which is transmitted by the corresponding function module 11 as the fifth byte in every telegram in the addressed function module 11 by dividing the first four bytes of the telegram, i.e. the address byte, the function byte, the first and the second data byte, continuously binarily through a polynomial generator g(z)=z.sup.8 +z.sup.7 +z.sup.2 +1. The CRC generator 80 receives the STRTN and CRE signals from the control device 83 (see FIG. 10) via control bus 96. When the starting conditions have been met the STRTN signal resets the shift register 211 to zero, whereupon the bits of the first four bytes of the telegram are pushed time-sequentially in to the shift register 211 by means of the 4-MHz clock signal, while the four bytes are divided binarily by means of the feedback from 211 via the exclusive-OR gates of the adders 212, 213 and 214 by the polynomial generator g(z). If no monitoring error exists, i.e. if the MF signal has a logic value "0", and when the T2 signal has a logic value "1", a logic value "1" appears at the output of the AND gate 107 (see FIG. 10) as a CRE signal triggering the evaluation of that bit which is appearing at that moment at the input of the CRC generator. At the parallel output of the shift register 211 and thereby on the bus 80a the calculated CRC byte then appears upon completion of the fourth byte of the telegram.

Detailed Description Text (125):
As mentioned earlier, the multiplexer 65a and the CRC generator 65b of the interface circuit 21 of the control module 10 are similar in structure to the multiplexer 81 and the CRC generator 80 of the interface circuit 25 of the function module 11, whereby the ER signal assumes the role of the CRE signal, the CLK clock signal that of the 4-MHz clock signal and the CLR reset signal the role of the STRTN signal (see FIG. 8). Similarly as in the function module 11, the bytes which are this time transmitted and received by the control module 10 are pushed in sequentially one after the other into the shift register of the CRC generator 65b and are continuously divided binarily by means of feedback by the same polynomial

generator g(z) which is also used in the function modules 11, with the difference that not four bytes, but all five bytes of the telegram, i.e. also the received CRC byte are binarily divided by the polynomial generator g(z) in the control module 10. In the absence of any transmission error the result of this binary division must be equal to zero at the end of the fifth byte, i.e. all the bits stored in the shift register of the CRC generator 65b must then be zero. Only in that case does a logic value "0" appear upon completion of the telegram at the output of the OR gate 65c (see FIG. 8) as an indication of error-free transmission. When a transmission error exists on the other hand, at least one bit in the shift register of the CRC generator 65b is other than zero, so that in that case a logic value "1" appears at the output of the OR gate 65c which functions as a decoder upon completion of the telegram, said logic value "1" being stored in the status register 62 to indicate an error in transmission and to trigger a repeat transmission.

Detailed Description Text (127):
When the function module 11 transmits one or several bytes, the bits of that byte, coming from the serial output of the shift register 69, reach sequentially one after the other a first input of the monitor-error detector 82 (see FIG. 9) directly on the one hand and, inverted via the output release gate 84, the conductor 36, the transmission unit 27, one of the two receiving units 28 and the conductor 35 (see FIG. 5) a second input of the monitor-error detector 82 on the other hand. The two input signals of the monitor-error detector 82 must therefore be different from each other. If this is not the case, a logic value "1" appears at the output of the non-exclusive OR gate 219 which is stored as an alarm in the flipflop 223 and appears as an MF signal at the output of the monitor-error detector 82 (see FIG. 20) when the MILD signal, which comes from the AND gate 163 (see FIG. 12) has a logic value "1". The MILD signal has a logic value "1" when the function module 11 is switched to transmission and the T1 signal has a logic value "1". The flipflop 223 has a locking means which is constituted by the OR gate 221. The STRTN signal resets the flipflop 223 at the beginning of each telegram to zero.

Detailed Description Text (128):
Just as each function module 11 monitors the bytes which itself transmits, the control module 10 also monitors those bytes which itself transmits and evaluates them by means of the monitor-error detector 64. The latter functions similarly to the monitor-error detector 82 of the function module 11, whereby the ES signal assumes the role of a MILD signal, the CLK clock signal the role of the 4-MHz clock signal and the CLR reset signal the role of the STRTN signal (see FIG. 8). If at least one monitored bit does not agree with the transmitted bits, a logic value "1" appears at the output of the monitor-error detector 64 and is readably stored in the status register 62 to interrupt the telegram and to initiate a repetition of the transmission. If a monitoring error occur during the transmission the telegram transmission is immediately interrupted in each instance and an ITR interrupt signal is triggered.

Detailed Description Text (129):
An error-free transmission recognized by the control module 10 during the CRC control as well as during the monitoring control is confirmed by the control module 10 after the end of the telegram in that it transmits a confirmation impulse "telegram O.K." on the conductors 29 and 30 of the CLK clock signal (see FIG. 5) after the fortieth clock impulse of the CLK clock signal by means of the EC signal and the AND gate 66a of the transmission unit 66 (see FIG. 8). This confirmation impulse comprises preferably that the start impulse is transmitted once more as a confirmation at the end of the telegram. In case of telegram with error(s) on the other hand, the control module transmits a confirmation impulse "telegram not O.K." on the conductors 29 and 30. Through this confirmation impulse the addressed function module 11 learns whether the telegram received was O.K. and only then definitely carries out the received commands which were stored in the meantime. The confirmation impulse "telegram not O.K." comprises preferably that the so-called

"time-out" period is awaited at the end of the telegram before transmission of a new start impulse via conductors 29 and 30.

Detailed Description Text (130):
Simultaneously with the confirmation signal "telegram O.K.", the registers 58 to 61 (see FIG. 8) in the control module 10 whose writing was locked during the transmission of the telegram are again released for a writing process and the ITR Interrupt signal is triggered. Lastly, through a following reading of the status register 62, it is returned to null (i.e. zero).

Detailed Description Text (135):
The first variant of the output circuit 44 shown in FIG. 23 comprises several, e.g. four tri-state transmitters 235 and of as many tri-state receivers 236. The output bus 86 of the interface circuit 25 is connected to the inputs of the tri-state receivers 236 the outputs of which are connected to the inputs of the tristate transmitters 235 and are at the same time connected to the cable connection 13 which is shown in form of bus in FIG. 23. The outputs of the tri-state transmitters 235 are carried to the input bus 85 of the interface circuit 25. The control inputs of the tri-state receivers 236 are connected two by two for example, and each is connected to one of the two control circuits 87 or 88.

Detailed Description Text (136):
The data put at the disposal of the technical operating installation 9 or the data it makes available are either digital or analog data. In the first instance, the output circuit 44 of the function module 11 has the structure shown in FIG. 23. The digital data coming from the interface circuit 25 and going over the latter's output bus 86 reach the tri-state receivers 236 which are released in the presence of a write cycle by the signals appearing on the control circuits 87 and 88 and which amplify the data signals, so that the latter reach the cable connection 13 and beyond same the technical operating installation 9 in an amplified state. When a read cycle applies, the digital data coming from the technical operating installation 9 go over the cable connection 13, the always released tri-state transmitters 235 and the input bus 85 to reach the interface circuit 25 where they undergo further processing.

Detailed Description Text (137):
The second variant of the output circuit 44 of the function module 11 shown in FIG. 24 comprises a demultiplexer 237 and of two channels 238 and 239 for example, whereby each channel 238 and 239 contains a digital/analog converter 240 and for each of these an amplifier 241 downstream of same which are connected in the indicated sequence in series within each channel 238 and 239. The output bus 86 of the interface circuit 25 is connected to the input of the demultiplexer 237 the first bus output of which is connected via a bus to the input of channel 238 and the second bus output of which is connected via an additional bus to the input of channel 239. Each of the outputs of the amplifiers 241 constitutes an output of the output circuit 44 and is connected to the cable connections 13.

Detailed Description Text (139):
The third variant of the output circuit 44 of the function module 11 shown in FIG. 25 comprises bridges or shunts 242, for example two in number, which are used only optionally, of a multiplexer 243, an optionally used filter 244, an also optionally used amplifier 245, an analog/digital converter 246, a demultiplexer 247 and two writing registers 248 and 249. Two cable connections 13, each of which constituting an analog-value channel, are both connected via the bridges or shunts 242 to an input of the multiplexer 243 whose output is connected in the sequence indicated via filter 244 and amplifier 245 to the analog input of the analog/digital converter 246 whose digital output is again connected via a bus to the input of the demultiplexer 247. A first bus output of the demultiplexer 247 is connected to the parallel input of the shift register 248 and a second bus input of the demultiplexer 247 is connected to the parallel input of the shift register 249. The

parallel outputs of the two shift registers are connected in parallel and are connected to the input bus 85 of the interface circuit 25.

Detailed Description Text (142):
The write cycle of a data telegram as shown in FIG. 26 preferably comprises five bytes I to V, of which the first four bytes I to IV are transmitted from the control module 10 operating as "master" M to the function module 11 which operates as a "slave" S. Only after the reception of these first four bytes I to IV does the function module 11 transmit the fifth byte in form of CRC byte to the control module 10.

Detailed Description Text (143):
The read cycle of a data telegram shown in FIG. 27 preferably comprises also of five bytes I to V of which this time only the first two bytes I and II are transmitted from the control module 10, operating again as a "master" M, to the function module 11 which again operates as a "slave" S. Only following the reception of these first two bytes I and II does the function module 11 transmit the last three bytes of the telegram to the control module 10.

Detailed Description Text (145):
The embodiment of the drive of a technical operating installation 9 shown in FIG. 28 contains an output circuit 44 of the function module 11 and a partial circuit of the technical operating installation 9. In practice the technical operating installation 9 contains of course a plurality of partial circuits which are similar to or also different from the partial circuit shown in FIG. 28. In FIG. 28 only one single partial circuit was shown in order to explain the functioning of the output circuit 44 in a simple manner and in detail. It is therefore provided with minimum equipment in FIG. 28, i.e. with a 1-bit output and a 1-bit input so that only one single tri-state transmitter 235 and one single tri-state receiver 236 are used. The tri-state receiver 236 can be a commercially obtainable CMOS reception driver 250, for example, comprising a transistor 251 which can be a bi-polar NPN transistor and of a relay 252 which is provided with a relay coil 253 and with a relay contact 254. The relay contact 254 can be a closing contact, for example. The output bus 86 of the interface circuit 25 comprises in FIG. 28 of only one single bus connector 86 which is connected to the input of the CMOS reception driver 250 whose control input is for example connected to the control circuit 87 and whose output is connected to the base of transistor 251. If the CMOS reception driver 250 has an open collector output, the transistor 251 is of course not necessary since it is already contained in the CMOS reception driver 250. In that case the output of the CMOS reception driver 250 can be connected directly to the coil 253. The emitter of the transistor 251 is connected to the conductor 41, i.e. it is connected to the system ground GO. The collector of the transistor 251 is connected to the conductor 40, i.e. to the potential BEZ via relay coil 253. In practice an AC voltage V5 and/or V6 is also required to supply drives and other power consumers. The AC voltages V5 and V6 are preferably connected via function module 11. The AC voltage V5 has preferably a value of 24 volt and the AC voltage V6 a value of 220 volt in Europe or 110 volt in the USA. A pole of the AC voltage V5 is connected to the conductor 41 and thereby to the system ground GO. The AC voltage V5 supplies via relay contact 254 a coil 255 of a relay 256 of the technical operating installation 9 for example, whose power current contact 257 can switch a single-phase motor 258 on or off for instance, said motor in turn being used to drive a pump or a mixing valve for example. To achieve this, the AC voltage V6 supplies the single phase motor 258 via the power current contact 257. The relay 256 also has an auxiliary contact 259 whose position is reported via the tri-state transmitter 235 of the function module 11 and via the input bus 85 of the interface circuit 25 to the control module 10. In the drawing of FIG. 28 the output circuit 44 of the function module 11 has only one single tri-state transmitter 235 and the input bus 85 of the interface circuit 25 has only one single bus conductor 85. The tri-state transmitter 235 can comprise commercially obtainable CMOS transmission driver 260 and of a resistor 261. The system ground GO is connected via auxiliary

contact 259 of the relay 256 to an input of the CMOS transmission driver 260 and to a first pole of the resistance 261, the second pole of which is connected to the positive pole of the 5-volt supply distribution voltage of the function module 11. The output of the CMOS transmission driver 260 is connected to the single bus conductor 85 of the input bus 85 of the interface circuit 25.

Detailed Description Text (146):
In the circuit shown in FIG. 28 the technical operating installation 9 receives a digital 1-bit data value from the control module 10 via the CMOS reception driver 250, the transistor 251 and the relay 252, whereby the relay contact 254 of the latter switches the coil 255 of the relay 256 on or off by means of the AC voltage V5, depending on whether a logic value "1" or "0" has been emitted from the control module. The high voltage contact 257 of the contactor 256 then switches the single-phase motor 258 on or off by means of the AC voltage V6. The ON or OFF position of the relay 256 is then reported back by means of its auxiliary contact 259 via the CMOS transmission driver 260 of the function module 11 to the control module 10. It should be noted that the switching currents of the coil 255 of the contactor 256 flow over the system ground GO and can cause non-negligible ohmic and/or inductive voltage drops in these which would interfere with the transmission of the telegram if the voltages of their transmission signals DA and CLK were referred to the system ground GO. A mentioned earlier, this is avoided in that this voltage is referred to the potential BEZ of the conductor 40 and not to the potential GO of the conductor 41 (see FIG. 5).

Detailed Description Text (157):
In a very universal ZLT building automation system according to the instant invention the wiring, terminal, connections and assembly costs within the control cabinet have been reduced to a minimum and costly shunt wiring is not necessary since the connections of the technical operating installation are not connected to terminals 283; 285 but directly to the connections 276 of the function modules 11. This makes it possible to save much time and money. Because the function modules can be plugged in at any location on a bus rail without consideration for their own function module type and without consideration for the function module type which may have been plugged in earlier at the same location optimal flexibility of the installation is ensured with respect to modification and expansion of the system thanks to the unlimited possibility to replace the function modules 11. By using the BEZ potential instead of the GO potential as a common reference potential for the transmission signals DA and CLK a reduction of the tendency for errors is achieved in the installation because a transmission connection with a lower tendency for errors exists between the control module 10 and the function modules 11. By reducing the number of conductors in the bus rail 12 to four to seven conductors and by using an optimally thin cable-bus connection 14 between the bus rail 12 and the control modules 10, it is possible to install the latter on the door of the control cabinet or control panel instead of on the bus rail 12. In this way the control and display elements of the control module 10 are accessible directly from the outside without need to open the door first. Due to the fact that the start-up and the testing of the installation for the presence of wiring mistakes is very much simplified, mainly thanks to the presence of the bus connection 12; 14, a reduction of the number of sources of errors can be expected. For the same reason the planning in setting up wiring diagrams, wire laying lists etc. is simplified considerably. Other advantages are great installation and maintenance friendliness, small space requirements for a high degree of useability of the installation as well as the reduction of the number of cable wiring harness produced in the field. Since the conversion of the analog values into digital values occurs already in the function modules 11 it takes place in a matter of seconds and at the same time relieves the mainframe computer of time-consuming conversion tasks.

CLAIMS:

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1. A building automation system comprising in combination

an arrangement located in an housing (280) for supervision, control and regulation of said building automation system and

a technical operating plant (9) of said building automation system located outside of said housing (280) of said arrangement,

said arrangement comprising in combination

a control module (10) serving as master transmitter-receiver,

a bus rail (12) comprising a plurality of conductors (30, 32, 40, 41) and located remotely from said control module (10) at the electrical periphery of said arrangement, said bus rail (12) including a plurality of bus rail connector elements (273) which define positions along said bus rail (12),

one or more function modules (11) serving as slave transmitter-receivers installed in a row along said bus rail (12), each of said one or more function modules (11) having an adjustable address independent of their position along said bus rail (12), and

a bus connection (12;14) connecting electrically said control module (10) and said one or more function modules (11) for transmission of address signals, data signals and supply voltages, said bus connection (12; 14) including said bus rail (12), and wherein

each of said one or more function modules (11) includes a terminal block (274) and a separate electronics block (275),

said electronics block (275) being provided with a set of connector elements (279) for connecting said electronics block (275) interchangeably with any one of said bus rail connector elements (273) located at any one of said positions along said bus rail (12), so that the corresponding function module (11) is connected electrically to said plurality of conductors (30, 32, 40, 41) of said bus rail (12) via one of said connector elements (273), and

said terminal block (274) being provided with connection elements (276) for connecting electrically the corresponding function module (11) directly via separate cable connections (13) to a device of said technical operating plant (9) for transmission of process parameters of said technical operation plant (9),

wherein said bus connection (12; 14) includes a cable connection (14) located between said control mode (10) and said bus rail (12), and

wherein said arrangement further comprises at least one feed module (15) which is electrically plugged in on said bus rail (12) via one of said bus rail connector elements (273) to establish an electrical connection between said cable connection (14) and said bus rail (12).

2. The building automation system in accordance with claim 1, wherein said address signals and said data signals are arranged sequentially in telegram signals transmitted between said control module (10) and each of said one or more function modules (11).

3. The building automation system in accordance with claim 2, wherein one of said telegram signals comprises at least one address byte and at least one data byte, whereby during a write cycle said address and at least one data bytes are transmitted from said control module (10) to said one or more function modules (11), and whereby during a read cycle said address byte is transmitted from said

control module (10) to said one or more function modules (11) and said at least one data byte is transmitted from one of said one or more function modules (11) to said control module (10).

4. The building automation system in accordance with claim 2, wherein one of said telegram signals comprises at least one address byte, one function byte and at least one data byte, whereby during a write cycle all of said byte are transmitted from said control module (10) to said one or more function modules (11), and whereby during a read cycle said address and function bytes are transmitted from said control module (10) to said one or more function modules (11) and said at least one data byte is transmitted from one of said one or more function modules (11) to said control module (10).

5. The building automation system in accordance with claim 2, wherein one of said telegram signals comprises at least one address byte, at least one data byte and one CRC byte, whereby during a write cycle said address and at least one data bytes are transmitted from said control module (10) to said one or more function modules (11) and said CRC byte is transmitted from one of said one or more function modules (6) to said control module (10), and whereby during a read cycle said address byte is transmitted from said control module (10) to said one or more function modules (11) and said CRC and at least one data bytes are transmitted from one of said one or more function modules (11) to said control module (10).

6. The building automation system in accordance with claim 2 wherein one of said telegram signals comprises at least one address byte, one function byte, at least one data byte and one CRC byte, whereby during a write cycle said address, function and at least one data bytes are transmitted from said control module (10) to said one or more function modules (11) and said CRC byte is transmitted from one of said one or more function modules (11) to said control module (10), and whereby during a read cycle said address and function bytes are transmitted from said control module (10) to said one or more function modules (11) and said CRC and at least one data bytes are transmitted from one of said one or more function modules (11) to said control module (10).

7. The building automation system in accordance with one of claims 3-6 wherein said telegram signals comprise two data bytes.

8. The building automation system in accordance with claim 1, wherein said bus connection (12;14) includes a conductor for the transmission of a clock signal.

9. The building automation system in accordance with claim 8 wherein said arrangement includes a common potential (GO) to which voltages inside of said control module (10) and of said technical operating plant (9) are referred, wherein said bus connection (12;14) includes a pair of conductors (40, 41) for transmitting a DC voltage, a first of the conductors (41) of said pair of conductors (40, 41) being connected to said common potential (GO), and wherein the voltages of said address, data and clock signals transmitted via said bus connection (12;14) are referred to the potential of the second conductor (40) of said pair of conductors (40, 41) rather than to the potential of the first conductor (41).

10. The building automation system in accordance with claim 9, wherein said control module (10) comprises at least one level adaptation circuit (20), including a transmission circuit (23), said transmission circuit (23) being supplied by a DC voltage source (39), the first pole of which is connected to said second conductor (40) of said pair of conductors (40, 41) and the second pole of which is connected to a supply pole of said transmission circuit (23).

11. The building automation system in accordance with claim 9, wherein said bus rail (12) is provided with two conductors for the distribution of an AC voltage (V6), said two conductors being connected via a feed module (15) each to a

conductor (263, 264) of a cable connection.

12. The building automation system in accordance with claim 9, wherein said bus rail (12) is provided with an additional conductor for the distribution of a first AC voltage (V5) whereby one pole of the first AC voltage is connected to the first conductor (41) of said pair of conductors (40, 41) and whereby said additional conductor of said bus rail (12) is connected via a feed module (15) to a conductor (262) of a cable connection.

13. The building automation system in accordance with claim 1, wherein said one or more function modules (11) and said control module (10).

14. The building automation system in accordance with claim 13, wherein said control module (10) includes an interface circuit (21) associated with said digital circuit and at least one adaptation circuit (20) downstream of said interface circuit (21), said at least one level adaptation circuit (20) comprising a first transmission circuit (23) for a clock signal, a second transmission circuit (23) for a data signal and a receiving circuit (24) for a signal, and wherein each of said function modules (11) includes an adaptation circuit (26) at the input thereof and comprising a transmitting circuit (27) for a data signal, a first receiving circuit (28) for a clock signal, and a second receiving circuit (28) for a data signal.

15. A building automation system comprising in combination

an arrangement located in an housing (280) for supervision, control and regulation of said building automation system and

a technical operating plant (9) of said building automation system located outside of said housing (280) of said arrangement,

said arrangement comprising in combination

a control module (10) serving as a master transmitter-receiver,

one or more function modules (11) serving each as a slave transmitter-receiver, and

a bus connection (12;14) including a bus rail (12) for connecting electrically said control module (10) and said one or more function modules (11) for the transmission of address signals and data signals and the transmission of supply voltages, and

wherein said bus rail (12) is installed remotely from said control module (10) at the electrical periphery of said arrangement, and

wherein said bus rail (12) is comprising a plurality of conductors (30, 32, 40, 41) and a plurality of bus rail connector elements (273) which define positions along said bus rail (12), and

wherein each of said one or more function modules (11) includes a terminal block (274) and an electronics block (275),

said electronics block (275) being provided with a set of connector elements (279) for connecting said electronics block (275) interchangeably with any one of said bus rail connector elements (273) located at any one of said positions along said bus rail (12), sot hat the corresponding function module (11) is connected electrically to said plurality of conductors (30, 32, 40, 41) of said bus rail (12) via one of said connector elements (273), each of said one or more function modules (11) having an adjustable address independent of their position along said bus rail (12), and

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said terminal block (274) being provided with connection elements (276) for connecting electrically the corresponding function module (11) directly via separate cable connections (13) to a device of said technical operating plant (9) for transmission of process parameters of said technical operating plant (9), and

wherein said control module (10) includes a digital circuit controlled by a microcomputer (50) for controlling transmission between said one or more function modules (11) and said control module (10), and

wherein said microcomputer (50) is connected to an address memory (52) and to a bi-directional data driver (53), and wherein said arrangement further comprises a direction control device (54) for determining the direction of transmission of the bi-directional data driver (53), and

wherein said digital circuit contains an address register (58) for storing an address byte, a function register (59) to store a function byte if one is to be transmitted, at least one data register (60 or 61) to store a data byte, a status register (62) to store a status of said arrangement, a shift register (63) serving as a parallel/serial or serial/parallel converter, a transmitting unit (66) and a receiving unit (67), whereby all the registers (58, 59, 60, 61, 62) are connected to the address memory (52) and to the bit-directional data driver (53) and whereby all the registers (58, 59, 60, 61) with the exception of the status register (62) are connected to a parallel input/output of the shift register (63) whose serial output is connected via the transmitting unit (66) to the input of a transmission circuit (23) of a level adaptation circuit (20), while an output of a receiving circuit (24) of said level adaptation circuit (20) is connected via the receiving unit (67) to a serial input of the shift register (63).

16. The building automation system in accordance with claim 15, wherein said digital circuit contains a CRC generator (65b), wherein the output of the receiving unit (67) is connected to an input of a multiplexer (65a) and an output of the transmitting unit (66) is connected to another input of said multiplexer (65a), the output of said multiplexer (65a) being connected to a signal input of said CRC generator (65b), said CRC generator (65b) having parallel outputs connected to the inputs of a decoder (65c), the output of said decoder (65c) being connected to an input of the status register (62).

17. The building automation system in accordance with claim 15 or claim 16 wherein said digital circuit further comprises a monitor-error detector (64) to evaluate the bytes emitted from the control module (10) which go from an output of the transmitting unit (66) over two different paths, each to an input of the monitor-error detector (64), whereby an output of the transmitting unit (66) is connected to one input of the monitor-error detector (64) and the output of the transmitting unit (66) is connected to an input of the level adaptation circuit (20) and the output of a receiving circuit (24) of said level adaptation circuit (20) is connected to another input of the monitor-error detector (64) whose output is carried to an input of the status register (62).

18. The building automation system in accordance with claim 15, wherein an interface circuit (25) is installed in each of the one or more function modules (11) and is provided with an input bus (85) which is connected to a parallel input of a shift register (69) whose parallel output in turn is connected to a bus input of an address comparator (71) which serves to compare a received address with a modular address stored in an address coder (72), to a bus input of a function decoder (73) if a received function byte is evaluated and to a bus input of an output stage (74), whereby the address coder (72) is connected to an additional bus input of the address comparator (71) and a data bus output of the output stage (74) is connected to an output bus (86) of the interface circuit (25), and in that said interface circuit (25) further comprises a control device (83) as well as an output

release gate (84), whereby a serial output of the shift register (69) is connected via the release gate (84) to the input of a transmission circuit (27) of an adaptation circuit (26) and the output of a receiving circuit (28) of the adaptation circuit (26) is connected to a serial input of the shift register (69).

19. The building automation system in accordance with claim 18, wherein the interface circuit (25) of each of the one or more function modules (11) contains a random code generator (77) for the control of a multiple occupation of modular addresses and a module information coder (78) for the adjustment of module information and in that the random code generator (77), the module information coder (78) and the input bus (85) are each connected to a bus input of a bus multiplexer (70) whose output is connected to the parallel input of the shift register (69).

20. The building automation system in accordance with claim 19, wherein when a CRC byte transmission occurs the interface circuit (25) of each of the one or more function module (11) contains a multiplexer (81) whose output is connected to a serial input of a CRC generator (80) serving to produce a CRC byte, whereby a serial input and a serial output of the shift register (69) are each connected to an input of the multiplexer (81) and in that an output of the CRC generator (80) is connected via a bus (80a) to an additional bus input of the bus multiplexer (70).

21. The building automation system in accordance with claim 19 or claim 20, wherein the input bus (85) of the interface circuit (25) of the function module (11) is connected via an input filter (79) to the bus multiplexer (70).

22. The building automation system in accordance with claim 18 or claim 19 or claim 20, wherein the interface circuit (25) of the function module (11) contains a monitor-error detector (82), whereby the serial input an the serial output of the shift register (69) are each connected to an input of the monitor-error detector (82).

23. The building automation system in accordance with claim 18 or claim 19 or claim 20, wherein the output stage (74) of the interface circuit (25) of the function module (11) comprises a buffer memory (75) and an output register (76) connected to said buffer memory (75) by means of a bus (75a).

24. The building automation system in accordance with claim 1 or claim 15 wherein said terminal block (274) is provided with connector elements (277) for plugging in the electronics block (275), while the electronics block (275) in turn is provided with an additional set of connector elements (278) for plugging into the terminal block (274), whereby all connector and connection elements (273, 277, 278 and 279) of each of said one or more function modules (11) are installed in such manner that the electronics block (275) can be pulled out of the corresponding terminal block (274) and from the bus rail (12) nearly simultaneously without requiring dissassembly of the terminal block (274) or disconnection of the cable connection (13).

L2: Entry 6 of 9 File: USPT Oct 23, 2001

DOCUMENT-IDENTIFIER: US 6307958 B1
TITLE: Method and system for building a database for use with selective incentive marketing in response to customer shopping histories

Brief Summary Text (16):
Copending patent application Ser. No. 07/826,255 discloses a system and technique wherein a customer's checking account number may be used as a unique customer identification number to provide credit verification and also to perform marketing functions. In such a prior system, such customer checking account numbers have been manually entered by the retail store clerk, thus causing delay and possible inaccuracies. A need has thus arisen for an automated system for providing quick and efficient check verification and marketing follow-up. Previous automatic readers have, however, not been satisfactory for such purposes, because of their inability to uniformly detect desired account information on all checks in a consistent manner. Readers should also be able to read credit cards as well as checks.

Detailed Description Text (86):
EPROM 134 receives a 12-bit address A00-A12 from the Address Bus. The lower order bits A00-A07 are provided by address latch 132, and are available on the Address Bus during the second address cycle when the higher order bits A8-A12 are provided by microprocessor port 0 over the Address Bus. Thus, EPROM 134 receives the complete 12-bit address A00-A12 from the Address Bus during the second address cycle. The addressed data byte AD0-AD7 is available from the EPROM output port over the Address/Data Bus and may be read when microprocessor 130 provides a data strobe DS to the chip enable CE input to the EPROM.

Detailed Description Text (88):
LCD module 136 is enabled for output over the Address/Data Bus by an enable signal from a NOR gate 146, which receives input from the microprocessor's data strobe DS line and data memory DM line (port 3, pin 4). That is, LCD module 136 may be read only if both the data strobe and data memory lines are active. In contrast, EPROM 134 is enabled for a read operation only if the data strobe line is active while the data memory line is inactive causing an active output from an inverter 144. In this manner, microprocessor 130 uses the data memory line to select between program memory (EPROM 134) and data memory (LCD module 136).

Detailed Description Text (394):
While event frequency for a given activity is a matter of store policy and design choice, typically, host/remote communications and backup will be performed fairly frequently to insure both the regular update of the customer database, and the ability to recover from a system failure without significant loss of data. On the other hand, the purge function is more a matter of system administration designed to control the size of the customer database. Indeed, the purge function can be omitted as an event activity. In that case, the status purge limits contained in the system control file define the reset/CAUTION interval used in the roll routine to roll all statuses back to CAUTION if the specified reset/CAUTION (i.e., purge) limits are exceeded, as described in connection with FIG. 9B.

Detailed Description Text (471):

h e b b g e e e f c e e e ge

It may thus be seen that the program of FIGS. 15A and 15B provides an efficient technique of building a customer database and mailing list using checks from a variety of different banks. In operation, a customer's checking account identification number is detected by the check reader 119 for use as a unique customer identification code. As previously disclosed, a unique aspect of this invention is that the present check reader can determine checking account identification numbers even if the proper spacing and symbology is not utilized. The system can also detect changes in bank transit numbers. The checking account identification number is entered into processor 110 which contain a database that maintains customer records including the customer's name and address, the checking account identification number, and customer shopping habits and transactional data over a preselected time interval. The checking account identification number is compared with the database. A response is generated by the processor 110 to signal the presence of the customer's checking account identification number or the failure to locate the customer's checking account identification number. A new record is then created in the database for that customer's checking account identification number in response to a processor 110 response indicating the failure to locate, so that the customer's name and address is entered into the record along with a shopping incidence and shopping data being recorded in the database concurrently. A list of customers is then generated in the database whose last transaction date is prior to a preselected interval of inactivity so that grouping or subgrouping of customers is available for marketing efforts.

Detailed Description Text (485):
FIGS. 18A, 18B, and 18C illustrate a technique for generating coupons based upon the particular transaction currently being accomplished by the customer. The technique of FIGS. 18A, 18B, and 18C detects the particular store departments in which the products being purchased are located. This system requires the use of the bar code scanner to detect which products are being purchased, and which departments are being shopped by the customer. For example, the technique shown in FIGS. 18A, 18B, and 18C detects whether or not items have been purchased from the meat department, dairy department or deli. Based upon data stored within the computer, the decision is then made as to whether to award a coupon and what type of coupon to award. For example, if the data illustrates that over a period of time a shopper shows a consistent failure to shop at the delicatessen, then when the customer's check identification is scanned into the check reader 119, the processor 110 pulls up the customer's history and generates a coupon to induce the customer to shop at the delicatessen the next time the customer shops. This inducing can be done by providing the customer with a very high value coupon used only for deli shopping.

Other Reference Publication (23):
Lexis printout. An article by Antonia Feuchtwanger entitled "Smarter cards think for themselves in US tests" (hereinafter referred to as "the Feuchtwanger publication") was published in the Daily Telegraph on Nov. 2, 1990, p. 20.

L2: Entry 5 of 9 File: USPT Dec 25, 2001

DOCUMENT-IDENTIFIER: US 6334108 B1
TITLE: Method and system for selective incentive point-of-sale marketing in response to customer shopping histories

Brief Summary Text (16):
Copending patent application Ser. No. 07/826,255 discloses a system and technique wherein a customer's checking account number may be used as a unique customer identification number to provide credit verification and also to perform marketing functions. In such a prior system, such customer checking account numbers have been manually entered by the retail store clerk, thus causing delay and possible inaccuracies. A need has thus arisen for an automated system for providing quick and efficient check verification and marketing follow-up. Previous automatic readers have, however, not been satisfactory for such purposes, because of their inability to uniformly detect desired account information on all checks in a consistent manner.

Detailed Description Text (91):
EPROM 134 receives a 12-bit address A00-A12 from the Address Bus. The lower order bits A00-A07 are provided by address latch 132, and are available on the Address Bus during the second address cycle when the higher order bits A8-A12 are provided by microprocessor port 0 over the Address Bus. Thus, EPROM 134 receives the complete 12-bit address A00-A12 from the Address Bus during the second address cycle. The addressed data byte AD0-AD7 is available from the EPROM output port over the Address/Data Bus and may be read when microprocessor 130 provides a data strobe DS to the chip enable CE input to the EPROM.

Detailed Description Text (93):
LCD module 136 is enabled for output over the Address/Data Bus by an enable signal from a NOR gate 146, which receives input from the microprocessor's data strobe DS line and data memory DM line (port 3, pin 4). That is, LCD module 136 may be read only if both the data strobe and data memory lines are active. In contrast, EPROM 134 is enabled for a read operation only if the data strobe line is active while the data memory line is inactive causing an active output from an inverter 144. In this manner, microprocessor 130 uses the data memory line to select between program memory (EPROM 134) and data memory (LCD module 136).

Detailed Description Text (419):
While event frequency for a given activity is a matter of store policy and design choice, typically, host/remote communications and backup will be performed fairly frequently to insure both the regular update of the customer database, and the ability to recover from a system failure without significant loss of data. On the other hand, the purge function is more a matter of system administration designed to control the size of the customer database. Indeed, the purge function can be omitted as an event activity. In that case, the status purge limits contained in the system control file define the reset/CAUTION interval used in the roll routine to roll all statuses back to CAUTION if the specified reset/CAUTION (i.e., purge) limits are exceeded, as described in connection with FIG. 9B.

Detailed Description Text (498):
It may thus be seen that the program of FIGS. 15A and B provide an efficient

technique of building a customer database and mailing list using checks from a variety of different banks. In operation, a customer's checking account identification number is detected by the check reader 119 for use as a unique customer identification code. As previously disclosed, a unique aspect of this invention is that the present check reader can determine checking account identification numbers even if the proper spacing and symbology is not utilized. The system can also detect changes in bank transit numbers. The checking account identification number is entered into processor 110 which contain a database that maintains customer records including the customer's name and address, the checking account identification number, and customer shopping habits and transactional data over a preselected time interval. The checking account identification number is compared with the database. A response is generated by the processor 110 to signal the presence of the customer's checking account identification number or the failure to locate the customer's checking account identification number. A new record is then created in the database for that customer's checking account identification number in response to a processor 110 response indicating the failure to locate, so that the customer's name and address is entered into the record along with a shopping incidence and shopping data being recorded in the database concurrently. A list of customers is then generated in the database whose last transaction date is prior to a preselected interval of inactivity so that grouping or subgrouping of customers is available for marketing efforts.

Detailed Description Text (513):
FIGS. 18A, B, and C illustrate a technique for generating coupons based upon the particular transaction currently being accomplished by the customer. The technique of FIGS. 18A, B, and C detects the particular store departments in which the products being purchased are located. This system requires the use of the bar code scanner to detect which products are being purchased, and which departments are being shopped by the customer. For example, the technique shown in FIGS. 18A, B, and C detects whether or not items have been purchased from the meat department, dairy department or deli. Based upon data stored within the computer, the decision is then made as to whether to award a coupon and what type of coupon to award. For example, if the data illustrates that over a period of time a shopper shows a consistent failure to shop at the delicatessen, then when the customer's check identification is scanned into the check reader 119, the processor 110 pulls up the customer's history and generates a coupon to induce the customer to shop at the delicatessen the next time the customer shops. This inducing can be done by providing the customer with a very high value coupon used only for deli shopping.

Detailed Description Text (531):
In addition, it provides a barrier to physical participation because building a database with a card based system is a two step process, as opposed to a one step process when one employs customer ID based on transactionism. First of all, the customer has to sign up at the store because the name and address have to be recorded and usually merchants ask for additional demographic data. There are a large number of customers who regard that as an invasion of privacy and so are very reluctant to provide that sort of personalized information. Whereas on the transparent system of the present invention using ID's issued by a financial institution, there is no perceived invasion of privacy. Additionally, there is a barrier to participation by merchant cards caused by the need to constantly carry and constantly produce that ID at the point-of-sale. It has been the experience of most retailers that with respect to store cards, if customers can be induced to sign up at all, in very short order there is an enormous attrition because people lose them or they simply lose patience with the system with the slow-down at the point-of-sale. Over a period of time, the attrition rate for such merchant cards means that there is a continued drive and cost associated with that drive to resolicit people with the signup. Failure to get participation means that the data is less valid and that the participation from the standpoint of marketing intracity is dramatically reduced. So, the stores wind up having a small customer base that is contingent upon voluntary active participation of customers on the one hand,

versus near universal participation using the present system because it is invisible or transparent to the customer.

Detailed Description Text (558):
FIG. 27 illustrates the method of tracking infrequent shoppers such that a Coupon "A" may be generated by the high-speed point-of-sale printer 976. Coupon "A", as will be subsequently described, is defined as "coupons to incent what has been determined to be an infrequent shopper, that is a shopper who fails to meet predetermined shopping criteria". For example, criteria may be set of a predetermined number of shopping visits in a predetermined time. If the customer fails to meet the required number of shopping visits, he/she is determined to be an infrequent shopper and Coupon "A" may be used to incent that shopper. As will be subsequently described, Coupon "A" provides greater coupon incentives than are provided to customers who are more frequent shoppers. Although an infrequent shopper has been herein described as a customer failing to meet previous shopping criteria, the infrequent shopper may also be defined as a customer meeting predetermined infrequent shopping criteria, that is by not having visited a store in a predetermined time in a predetermined time interval. The flow chart in FIG. 27 also illustrates the generation of Super "A" Coupons to an infrequent shopper who has been previously targeted for marketing but has failed to respond. The steps include:

Detailed Description Text (595):
Once the system monitors a customer's subsequent activity, subsequent to the incentive, then the system can record the response. The system may then have a preset criteria of response and if that customer meets the preset response criteria, the system may either maintain that incentive over a preselected time interval or may initially or subsequently reduce that incentive over a preselected time interval. If the response criteria is favorably met, and the retail store is happy with the performance by the customer, then the store can either maintain or reduce or maintain and subsequently reduce the value of the incentive. On the other hand, if the customer fails to meet the response criteria, as is often the case, the incentive may be increased or changed.

Detailed Description Text (674):
The criteria for Super "A" will be the failure to redeem the coupon dispensed the prior week. The following Levels of Super "A" are set with each level providing incentives for 2 trips, as shown in Table 13.

Detailed Description Text (679):
Table 15 shows the initial offering to Household #1 and the following weeks of activity. Note the initial offering is 60.cent. OFF the 12 ounce package of BRAND A. This offering was arrived at based on the "Deal" indicated in Table 11 (40% OFF for Level 2) applied to the list price indicated in Table 12 ($1.50 for the 12 oz package) rounded to the nearest 5.cent.. It is important to note the difference between the Coupon "A" campaign for Household #2 vs Household #1. First, Household #2 had a lower PRODUCT TYPE consumption rate than Household #1 and therefore is being incented with the 12 oz package size rather than the 20 oz. Second, Household #2 had a lower percentage consumption of BRAND A vs PRODUCT TYPE and therefore received a higher incentive (40% OFF vs 25% OFF). In Household #2's campaign shown in Table 15, note that in week #2 this customer did NOT redeem the coupon dispensed in the prior week. This failure to respond to an incentive puts this customer's status to the first level of Super "A".

Detailed Description Text (680):
As indicated in Table 13, the first level of Super "A" results in an incentive equal to a 20% increase over the original incentive, or, in this case, 70.cent. OFF of the 12 oz package. In week #3, the customer once again fails to respond to the incentive and therefore moves to level 2 of Super "A" with a higher incentive of 85.cent. OFF of the 12 oz size. In week #4, the customer redeems the coupon and

receives another coupon for 85.cent. since this has proven to work. In week #5, the customer once again redeems the Super "A" coupon. This redemption results in the completion of Super "A" and the customer resumes the Coupon "A" program receiving the original incentive of 60.cent.. Weeks #6 and #7 result in redemptions, so the customer once again receives a coupon for 60.cent.. In week #8, however, this customer once again fails to respond to the incentive and once again begins the Super "A" campaign at level 1. This time, the first Super "A" coupon for 70.cent. is redeemed in week #9 but the second one is not redeemed in week #10 and therefore advances to level 2 once again with a Super "A" coupon for 85.cent.. This incentive once again proves sufficient for getting the customer to purchase BRAND A and once again falls back to Coupon "A" for week #12 and upon redemption in week #13, this Coupon "A" program is concluded.

Detailed Description Paragraph Table (30):
Step Description 106 Coupon "M" (for Maximize) is used by the system to track average expenditures and maintain a program for increasing customers' average purchases. Each store tailors criteria for increasing average purchases which are stored on-line as follows: Minimum number of trips to qualify for Coupon "M" program. This ensures that an account's history has matured so that a more accurate average may be obtained. Maximum dollar average to qualify for Coupon "M" program. This provides a ceiling to prevent attempts to increase average purchases that are considered sufficiently high. For example, if a customer has an average purchase of $125, it may not be reasonable to spool coupons incenting them to spend $135. Percentage to attempt increase in average purchase. Criteria for Super "M". This criteria is based on the failure to increase average purchases by a preset percentage of target increase. Number of trips before testing for Super "M" Coupons to be used for incenting the customer to increase spending. These coupons are tailored to the amount of the customer's target value (base average plus percentage increase). Each coupon contains a minimum target value in order to trigger spooling. For example, Customer A has an average base of $40. Assume a target increase of 10% to make a target of $44 rounded to $45. The first Coupon "M" incentive holds a minimum target value of $50. This coupon is NOT spooled. The second Coupon "M" incentive holds a minimum target value of $45. This coupon IS spooled with a minimum purchase qualifier of $45. The third Coupon "M" incentive holds a minimum target value of $30. This coupon IS spooled as well with a minimum purchase qualifier of $45. And so on for the rest of the Coupon "M" incentives all spooled with a minimum purchase qualifier of $45. Customer B has a target value of $35. For this customer, the first and second Coupon "M" incentives are not spooled because this target value does not meet the minimum. The third incentive with a $30 minimum target value IS spooled with a minimum purchase qualifier of $35. And so on with the rest of the Coupon "M" incentives as is done for Customer A, except now the minimum purchase qualifier will be $35. 107 As is done with Coupon "A", each account record holds fields for tracking coupon programs for Coupon "M". These fields include: Coupon "M" base. The base average arrived at when the program was initiated. Number of trips on Coupon "M" program. Super "M" flag to indicate account is in Super "M" program. Number of trips on Super "M" program. 108 If account is currently on a Super "M" program: 109 Calculate average purchase amount of purchases since beginning Super "M". 110 If average while on Super "M" exceeds preset criteria for percentage of increase of base, GOTO 121. 111 Mark account to receive Super "M" coupons. Increment Super "M" counter. GOTO 122. 112 If account is not currently in a Coupon "M" program: 113 If the number of trips does not meet the minimum trips specified to qualify for Coupon "M", GOTO 122. 114 Calculate a base average purchase amount for this account. Initialize fields for Coupon "M" in account's record to zeros and store base average. 115 If base average is greater than preset ceiling criteria, GOTO 122. 116 Calculate a target value by adding preset percentage increase of base to the base value. 117 Increment Coupon "M" program trip counter. If number of trips in Coupon "M" program is greater than or equal to preset criteria determining number of trips before testing results: 118 Calculate average purchases while on Coupon "M" program. 119 If average is less than preset criteria percentage increase for Super "M". GOTO 111 120 If average is

greater than target value, objective has been achieved. GOTO 122 121 Mark account to receive Coupon "M" Coupons. EXAMPLE: Customer makes a purchase. History shows this customer has made 11 purchases including this purchase. The preset criteria for minimum trips required to qualify for Coupon "M" is set to 10, so this customer now qualifies. Assume the average of these 11 purchases is $25. This is stored in the record as the base. The preset criteria for maximum base ceiling for Coupon "M" for this example is $50. This means any account with an average purchase of $50 or more does not qualify for Coupon "M". This account's average is less than $50 so the Coupon "M" tracking counters are set to zero and the program begins. Assume the preset percentage increase is 20%. A target is arrived at by adding 20% of the base to the base - in this case $25 + $5 or a $30 target. Coupons are spooled with a minimum purchase qualifier of $30 as described previously. Assume the preset value for number of trips before testing results is 5, then on the fifth trip an average is calculated for the trips since beginning Coupon "M", or in this case the last 5 trips. If in this example these last 5 trips averaged $35, the Coupon "M" program would be complete. If the average was still $25, and preset criteria to determine Super "M" specified that more than 50% of target increase should be achieved (in this case $27.50), then this account falls into Super "M".

Detailed Description Paragraph Table (47):
Step Description 1 Determine if this account is to receive incentives based on shopping history criteria pertaining to store visits, purchases to departments, purchases to a product group, or purchases to a single product. If account does not receive incentives, GOTO 8 2 Issue incentive and record incentive in customer record. 3 Monitor and record in customer record customer's response to incentive. 4 If a preset response criteria is met GOTO 6 5 Preset response criteria was not met. Incentive may be modified in response to failure to meet response criteria such as: Varying the value of the incentive Changing the conditional terms of the incentive Varying the product of the incentive (i.e. Offering cash discount versus merchandise) No modification, retry incentive GOTO 3. 6 Preset response criteria was met. Incentive may be modified in response to success in meeting response criteria such as: Reducing the incentive over preselected period of time so as to gradually taper off incentives Varying the product in order to accomplish same as above No modification maintain incentive over preselected period of time 7 If targeted marketing campaign is NOT complete, GOTO 3 8 END OF PROCESS

Detailed Description Paragraph Table (50):
TABLE 1 CUSTOMER RECORD DESCRIPTION Field Name Description char id [25]; /*customer's bank id */ unsigned long phone; /*customer's phone # for householding Digit 1 - multiple account flag Digit 2-8 - Phone # Digit 9-10 - Account counter */ struct { int hitcnt; /*total hitcnt */ long totamt; /*total cents amount verified */ long amount; /*last cents amount verified */ long dayamt [7]; /*Last 7 days cents verified */ long date; /*last verify access date/time */ } verify; struct { char status; /*current status */ char flags; /*id user flags */ long lastdate; /*last access date (for transfer use) */ long currdate; /*last access date (for rolling id) */ long statdate; /*date status changed */ }current; struct { unsigned daysago: 11; /*# days ago from last date (11 bits) */ unsigned hits : 5; /*Hits for that day (5 bits) */ unsigned amt; /*Amount in whole dollars */ }history [30] struct { char status; /*previous status before current */ int hitcnt; /*previous local hitcnt */ long totamt; /*previous local dollar amount */ long statdate; /*previous status date */ }previous; struct { unsigned int type; /*Bit Mask of coupons issued */ char flags; /*Miscellaneous coupon flags */ unsigned char Acntr;. /*Tally counters as Coupon "A"*/ unsigned char SAcntr; /*Tally counters as Super "A"*/ unsigned char Mcntr; /*Tally counters as Coupon "M"*/ unsigned char Mloop; /*Number of Maxxer loops */ unsigned char Floop; /*Number of failure loops */ unsigned int maxbase; /*Base avg for maxxing */ unsigned int suctarg; /*Last successful target */ char Slevel; /*Standard series run */ char Alevel; /*Coupon "A" Level */ }Coupon;

Detailed Description Paragraph Table (52):

h e b b g e e e f c e e e ge

TABLE 3 SYSTEM CONTROL FILE DESCRIPTION Field Definition char locid system id KpdPortDef keypad keypad definition int port modern comm port value int baud max baud rate of installed modern char tone tone/pulse dial mode long strttime system start time (machine turned on) long currtime current system time long timebomb timebomb date/time char errfile[FLNMSIZE] error filename char logfile[FLNMSIZE] screen log filename char password[LOCSIZE] system access password char privpass [LOCSIZE] privileged password (for tech) int timepass factor to change time password char flags system control flags char flags2 2nd set system control flags char CMS_flags1 future use CardLess flags char CMS_d flags2 another set of CardLess flags char dayflag flag for day/second roll limits long ctnroll caution to positive limit long ctnlim caution purge limit long neglim negative purge limit long poslim positive purge limit long colim cash only purge limit long sclim stolen purge limit VerifyLimit dmax day maximum call manager limits VerifyLimit wmax week maximum call manager limits VerifyLimit tmin total minimum call manager limits long break1 break value 1 for POS coupons long break2 break value 2 for POS coupons long break3 break value 3 for POS coupons int cms latest CardLess version making contact int collect latest ColleCheck version making contact int cvs current CVS version long set_date date counters were set to zero long to_date ending date for this set of counters Long couponA number qualifying for Coupon "A" Long amtA dollars Coupon "A" spent Long couponB number qualifying for Coupon "B" Long amtB dollars Coupon "B" spent Long couponC number qualifying for Coupon "C" Long amtC dollars Coupon "C" spent Long caution number of Cautions Long amt_caut dollars Cautions spent Long positive number of Positives Long amt_pos dollars Positives spent COUPON CONTROL DEFINITION char locid[10]; /*system id */ int flags; /*Bitwise flags for general coupon system */ int Issue; /*Bitwise flags for available check coupons */ int cash; /*Bitwise flags for available cash coupons */ struct { char det, /* How do we determine secondary shopper? 0 = Use $ vs Daylimits 1 = Use shopping frequency method */ int slim; /*$/trips less than this is Secondary Shopper */ char dlim; /*# of days/weeks for determination */ char avgdet; /*How do we determine A vs AA vs AAA? Using $ determination 0 = $ in last DayLimit days 1 = Weighted avg based on "n" trips 2 = Weighted avg based on $ in "n" weeks 3 = Weighted avg within last "n" days 4 = Mean avg based on "n" trips 5 = Mean avg based on $ in "n" weeks 6 = Mean avg within last "n" days 7 = Weeks attended in "n" weeks*/ int per; /*"n" trips/days/weeks to analyze avg $ */ char mintrp; /*Minimum # trips before det Secondary */ char high1; /*High $ in last "per" triggers AA,A */ char high2; /*High $ in last "per" triggers AAA,AA */ char high3; /*High $ in last "per" triggers 3A, 4A */ char high4; /*High $ in last "per" triggers 4A, 3A */ char perks; /*# trips for Secondary coupons */ char super_perks; /*# trips for Super Secondary */ char super_lag; /*# days before Super Secondary */ }Secondary; struct { char det; /*How do we determine Primary Status 0 = $ in last DayLimit days 1 = Weighted avg based on "n" trips 2 = Weighted avg based on $ in "n" weeks 3 = Weighted avg within last "n" days 4 = Mean avg based on "n" trips 5 = Mean avg based on $ in "n" weeks 6 = Mean avg within last "n" days 7 = Weeks attended in "n" weeks*/ char Limit; /*"n [trips/days/weeks for $ determination */ int CouponB; /*$ minimum for Coupon "B" */ int CouponC; /*$ minimum for Coupon "C" */ int CouponD; /*$ minimum for Coupon "D" */ int CouponE; /*$ minimum for Coupon "E" */ }Primary; struct{ char det; /* How do we determine avg 1 = Weighted avg based on "n" trips 3 = Weighted avg within last "n" trips 4 = Mean avg based on "n" trips 6 = Mean avg within last "n" trips unsigned char mbase; /*Maximum base for playing Maxxer */ unsigned char percent; /*Increase percent for Maxxing */ unsigned char loops; /*Number of passes at above percentage 0 = keep looping until failure */ unsigned char mintrp; /*Minimum # trips before using Maxxer */ unsigned char trips; /*# trips for establishing base avg */ unsigned char super; /*Number of trips til Super Max testing */ unsigned char mdur; /*Number of trips til give up Maxxer */ unsigned char Floops; /*Number of loops to retry failures */ char maxiflags; /*Maxxer Flags */ }Maxxer; struct{ long set_date; /*Date counters were set to zero */ long to_date; /*Ending date for this set of counters */ long hits [15]; /*Counters from Coupon "A1" to Coupon "E" */ long amts [15]; /*and Ctn's, Pos's, and No $ *A } counters[3]; /* 3 sets of cntrs; 2 for me */ struct{ long set_date; /* Start date for coupon Tracking */ long to_date; /* End date for coupon Tracking */ unsigned

h e b b g e e e f c e e e ge

int cntr [100]; /* Coupons issued for date range */ }CpnIssue[2] char Slevels; /* Number of standard series */ char Slags; /* Lag time before back to standard series 1 */ char Alags; /* Lag Time for Coupon "A" */ char BElags; /* Lag Time for Coupons "B"-"E" */ char maxissue; /* Max issued per trip */ char header[22]; /* Header for coupon */ char footer[29]; /* Footer for coupon */ long ResetDate; /* Date to reset standard issue lags */ int mpurchase; /* Minimum purchase */

Other Reference Publication (27):
Antonia Feuchtwanger "Smarter cards think for themselves in US tests" the Daily Telegraph on Nov. 2, 1990, p. 20.

CLAIMS:

16. The method of claim 15 and further comprising:

effecting a first sales promotion to said customer in response to said first signal;

monitoring said customer's shopping transactions subsequent to said first sales promotion;

generating with the processor a second signal in dependence upon the results of said monitoring of a customer whose shopping activity fails to meet a response criteria; and

effecting a subsequent second sales promotion to said customers whose shopping activity fails to meet said predetermined response criteria, said second sales promotion being differentiated from said first sales promotion.

First Hit Fwd Refs

End of Result Set

Generate Collection Print

L2: Entry 9 of 9 File: USPT Aug 2, 1988

DOCUMENT-IDENTIFIER: US 4761807 A
TITLE: Electronic audio communications system with voice authentication features

Detailed Description Text (18):
A single board computer 100 (hereinafter "SBC 100") operates as the central processing unit for the administrative subsystem 60, and it is implemented by a programmable single board computer, commercially available from Intel, Model No. 80/30. The SBC 100 has one input/output interface 102 connected to a cathode ray terminal (CRT) 104, which serves as the operator's console for the VMS10. The second input/output interface 106 of the SBC 100 drives a line printer 108. The line printer 108 functions to produce reports and status information concerning the operation of the VMS10, and it also displays alarms for abnormal conditions during the system operations. One such alarm condition would result from the failure of a recorded message to be transmitted from the VMS10 in a predetermined period of time.

Detailed Description Text (58):
The microprocessor 200 controls the ROM sequencer 290 by the three-bit command RA0, RA1 and RA3 which specifies the program function to be performed, setting a "0" in the RA3 bit which will release the ROM sequencer 290 by taking away the reset. When the ROM sequencer 290 finishes performing its function, it sets the "STOP" bit at the output latch 302 which the microprocessor circuit can sample through the RAM combination chip 202, and the ROM combination chip 206 responds by resetting the flip-flop 316, turning the ROM sequencer 290 off. The reset bit RSTM also serves as a fail-safe mechanism by allowing the ROM sequencer 290 only a certain amount of allotted time to perform its function. If too much time elapses, then the microprocessor circuit performs an error recovery procedure by unconditionally resetting the ROM sequencer 290.

Detailed Description Text (59):
The ROM sequencer 290 includes a bus cycle counter 318. The bus cycle counter 318 determines how many bus transactions have occurred by being incremented by the signal INCDMA every time a bus transaction occurs. By selecting a particular one of the Q outputs of the bus cycle counter 318, QA, QB, QC and QD, the counter can be adjusted to count by 2, 4, 6 or 8. Bus cycle counter 318 functions to prevent the ROM sequencer 290 from monopolizing time on the Intel bus when the ROM sequencer 290 is doing a bus block transfer. During a bus block transfer the ROM sequencer in effect locks out the other Universal Control Boards on that bus. Bus cycle counter 318 causes the ROM sequencer 290 to periodically give up control of the bus so that some of the Universal Control Board can use it. The output signal from the bus cycle counter 318 is the BUSCOUNT signal to one input of the input multiplexer 306.

Detailed Description Text (63):
As shown in FIG. 10g, cable timing control circuit 340 participates in the bus timing on the cable by originating one of the two signals on the cable and sampling the other. The signal DMAOUT is an output command signal generated by the cable timing control circuit 340 and the DMAIN signal originated on the cable bus driver

circuit. The BREADY signal is derived from the fourth output bit of the PROM 298 of the ROM sequencer 290 (FIG. 10f) and is connected to the inputs of NAND gates 342 and 344. A second input of the NAND gate 342 is connected to the WRITE signal from the ROM combination chip 206 and the WCZERO from the inverter 280 of the word count register 238. The output of the logic NAND gates 342 and 344 is fed through a NOR gate 346 to produce the READY output signal as one input to the D input of a D-type flip-flop 347. The flip-flop 347 has its Q output connected to one input of a three input NAND gate 348 and the clock input thereof connected to the ten megahertz clock. The NAND gate 348 also has its input tied to the DONE signal feed back from the output of the cable timing control circuit 340 and the DMACOMP signal from the output of the bus timing control circuit 540. (FIG. 10m). The output of the NAND gate 348 is fed through an inverter 350 to one pin of an input multiplexer 352. The input address of the multiplexer 352 is controlled by the state lines STB0, STB1 and STB2 as the output of a counter 354. Counter 354 essentially reflects the state of the cable timing control circuit 340. The input multiplexer 352 is sampling the DMAIN signal fed through flip-flop 356 which generates the output signals DMAINSY and DMAINSY as the inputs to multiplexer 352.

Detailed Description Text (68):
The data DB0-DB7 connected internally on the Universal Control Board moves through data bus 408 to command/status register of RAM combination I/O Chip 204 (FIG. 10b) and to the input of holding registers 410 and 412. The STROBE signal from the bus timing control circuit 540 (FIG. 10m) is fed through inverter 414 to the register 410. The INCDMA signal and READ signal are the inputs of NAND gate 416 having its output REN to the register 412. The REN signal is also fed through an inverter 418 and through one input of the NOR gate 406. The output of the NOR gate 406 is connected to the bus data drivers/receivers 400 and 402.

Detailed Description Text (73):
A bus address switch 450 is also connected to the IB0 cable bus 422 to provide an unique address for a Universal Control Board. The microprocessor circuit through its RAM combination chip 202 has an output signal RDSWT connected to the bus address switch 450 to read the preset switches which are the input to the bus address switch 450. The switch 450 has eight inputs labeled SW0, SW1, SW2, SW3, SW4, SW5, SW6 and SW7 referring to the number of switches present. By selectively grounding a combination of switches, an unique code can be manually placed into an individual Universal Control Board. This is part of the initialization function of the microprocessor circuit.

Detailed Description Text (76):
As shown in FIG. 10k, access to the bus is controlled by contention logic circuit 460. The contention logic circuit 460 is controlled by three signals, BUSY and BPRN from the bus and BUSREQfrom the ROM sequencer 290. The BUSY signal is an indication that the bus is busy with a transaction in progress. The BPRN signal is an indication of whether or not the Universal Control Board has priority. The BUSREQ signal is generated by the ROM sequencer 290 when it is doing either signal or block mode transfers. The OVERRIDE signal is from an input/output port of the ROM input/output port chip 206. A bus request flip-flop 462 may be set by either the BUSREQ or the OVERRIDE signal. The BUSREQ signal is fed through an inverter 464 to one input of a NOR gate 468 having its second input terminal tied to the OVERRIDE signal. The output of NOR gate 468, SBREQ, sets the bus request flip-flop 462. The BREQ signal from the output of the flip-flop 462 is fed through inverter 470 to appear as the signal BREQ which goes on the bus to some external logic which will arbitrate bus priority. This external controller determines priority and upon receipt of priority for the requesting Universal Control Board the BPRN signal is received by the control board and fed through inverter 472 to one input terminal of NAND gate 474. The BREQ signal is fed back through the output of the bus request flip-flop 462 to another input gate of the NAND gate 474. When the bus is no longer busy, the BUSY signal is fed through an inverter 476 and inverter 478 to the third input terminal of NAND gate 474. The output of NAND gate 474 is the output signal

SCON fed through an inverter 480 to set a connect flip-flop 482. The output connect signal is fed back through inverter 484 to generate the BUSY signal. The only way to reset the bus request flip-flop 462 is for the bus request signal to be reset. A BUSCLK signal is received from the bus and fed through an inverter 486 as the bus clock signal to the bus request flip-flop 462 and the connect flip-flop 482. The connect flip-flop 482 has an override circuit 487 attached to the input thereof. The override circuit generates the signal CONOVRIDE to connect a pullup to the flip-flop 482.

Detailed Description Text (77):
shown in FIG. 10-1, an address decode circuit 490 functions to decode the addresses AA0-AA7 from address drivers 262 and 264. Address signals AA4-AA7 are fed through address decoders 492 and 494 to generate output signal BDSEL, the board select signal. The other four signals AA3-AA0 are fed through address decoder 496 to select one of three functions on the board. The input/output reset function, the IORST signal, is fed through an inverter 498 to one input terminal of NAND gate 500. The other input of NAND gate 500 is from the IOW signal from the bus timing control circuit 540. The input/output reset function indicates that some other controller on the bus desires this Universal Control Board to be reset, and the IORST signal is fed to the reset circuitry 210 described hereinabove.

Detailed Description Text (80):
A third function of the address decoder 496 is an output fed through both input terminals of NAND gate 508 which has its output applied as one input to NAND gate 510. The outputs of NAND gates 506 and 510 are fed to the inputs of OR gate 512 which has its output connected to the input of NAND gate 514 which has its output connected to a data bus interface device 516.

Detailed Description Text (82):
A bus slave timing circuit 520 receives the strobes IOWC and IORC from the output of the bus timing control circuit 540. The IOWC signal is fed through inverters 522 and 524 to one input of OR gate 526. The IORC signal is fed through inverters 528 and 530 to the other input of OR gate 526. The output of OR gate 526 is input to shift register 532 to generate an output XACK fed through an inverter 534 to be conditioned as the signal XACK. The XACK signal is an acknowledgement to the bus that read and write strobes have been detected and the board select address has been detected. The board select signal is fed through an inverter 536 to the shift register 532. Shift register 532 also has a clock signal, CCLK, fed through an inverter 538.

Detailed Description Text (87):
The AND gate 564, having one input terminal connected to the output of AND gate 554, has a second input terminal connected to the IOCY signal from the RAM combination I/O chip 202. The output of AND gate 564 is fed to input terminals of AND gates 574 and 576. The second input terminal of the AND gate 574 is the READ signal, and the second input terminal of the AND gate 576 is the WRITE signal. The output of AND gate 574 is fed through an inverter 578 and is the IOWC signal used as an input to the bus slave timing circuit 520. The output of the AND gate 576 is fed through an inverter 580 which has as its output the IORC signal used as another input to the bus slave timing circuit 520.

Detailed Description Text (266):
CMDW, STATR, and STAT signals are input to a three-input NOR gate 1309. The output of the NOR gate 1309 is input to an inverter 1310 the output of which provides the BUS 1 SEL signal. The use of the BUS 1 SEL signal provides a further multiplexing function that will be described hereinbelow.

Detailed Description Text (269):
A NOR gate 1324 has one input thereof connected to the RD signal and the other input thereof connected to the WR signal. A NOR gate 1326 has one input thereof

connected to the DMA acknowledge signal for channel 0 (DACK0) and the other input there of connected to the DMA acknowledge signal for channel 1 (DACK1). A NAND gate 1328 has one input thereof connected to the output of the NOR gate 1324 and the other input thereof connected to the output of the NOR gate 1326. The output of the NAND gate 1328 provides the BUS 2 SEL signal for controlling the chip select input of the multiplexers 1314 and 1318. The gates 1324-1328 therefore comprise the circuitry that controls the multiplexers 1314 and 1318.

Other Reference Publication (1):
"An Automatic System for Verification of Cooperative Speakers Via Telephone", H. Ney et al., Proc. of 1981 Conf. on Crime Countermeasures, Univ. of Kentucky, Lexington, May 13-15, 1981, pp. 97-101.

Other Reference Publication (8):
"Petition for Waiver of American Telephone & Telegraph Company," before the Federal Communications Commission, Mar. 20, 1981.

Other Reference Publication (9):
"Reply Comments and Omnibus Motion of ECS Telecommunications, Inc. to petition for Waiver of American Telephone & Telegraph Company," by Ray Desing, 5/14/81.

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Search Results - Record(s) 1 through 9 of 9 returned.

☐ 1. Document ID: US 6684195 B1

Using default format because multiple data bases are involved.

L2: Entry 1 of 9 File: USPT Jan 27, 2004

US-PAT-NO: 6684195
DOCUMENT-IDENTIFIER: US 6684195 B1

TITLE: Method and system for selective incentive point-of-sale marketing in response to customer shopping histories

DATE-ISSUED: January 27, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Deaton; David W.	Abilene	TX		
Gabriel; Rodney G.	Abilene	TX		

US-CL-CURRENT: 705/14

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 6424949 B1

L2: Entry 2 of 9 File: USPT Jul 23, 2002

US-PAT-NO: 6424949
DOCUMENT-IDENTIFIER: US 6424949 B1

TITLE: Method and system for selective incentive point-of-sale marketing in response to customer shopping histories

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 3. Document ID: US 6377935 B1

L2: Entry 3 of 9 File: USPT Apr 23, 2002

US-PAT-NO: 6377935
DOCUMENT-IDENTIFIER: US 6377935 B1
** See image for Certificate of Correction **

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TITLE: Method and system for selective incentive point-of-sale marketing in response to customer shopping histories

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

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☐ 4. Document ID: US 6351735 B1

L2: Entry 4 of 9 File: USPT Feb 26, 2002

US-PAT-NO: 6351735
DOCUMENT-IDENTIFIER: US 6351735 B1

TITLE: Check transaction processing, database building and marketing method and system utilizing automatic check reading

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

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☑ 5. Document ID: US 6334108 B1

L2: Entry 5 of 9 File: USPT Dec 25, 2001

US-PAT-NO: 6334108
DOCUMENT-IDENTIFIER: US 6334108 B1

TITLE: Method and system for selective incentive point-of-sale marketing in response to customer shopping histories

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

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☐ 6. Document ID: US 6307958 B1

L2: Entry 6 of 9 File: USPT Oct 23, 2001

US-PAT-NO: 6307958
DOCUMENT-IDENTIFIER: US 6307958 B1

TITLE: Method and system for building a database for use with selective incentive marketing in response to customer shopping histories

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

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☑ 7. Document ID: US 6292828 B1

L2: Entry 7 of 9 File: USPT Sep 18, 2001

US-PAT-NO: 6292828
DOCUMENT-IDENTIFIER: US 6292828 B1

TITLE: Trans-modal animated information processing with selective engagement

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Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☑ 8. Document ID: US 5128855 A

L2: Entry 8 of 9 File: USPT Jul 7, 1992

US-PAT-NO: 5128855
DOCUMENT-IDENTIFIER: US 5128855 A

TITLE: Building automation system operating installation control and regulation arrangement

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☑ 9. Document ID: US 4761807 A

L2: Entry 9 of 9 File: USPT Aug 2, 1988

US-PAT-NO: 4761807
DOCUMENT-IDENTIFIER: US 4761807 A

TITLE: Electronic audio communications system with voice authentication features

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ Generate Collection Print

L5: Entry 1 of 1 File: USPT Jul 4, 1989

DOCUMENT-IDENTIFIER: US 4845594 A
** See image for Certificate of Correction **
TITLE: Reclosing relay with nonvolatile memory of operations

Detailed Description Text (28):
If the breaker CB does not close within a settable time period called Reclose Fail Time after a command to reclose has been sent by closing the K1 contacts, the reclosing relay 61 locks out, opens the reclose output contacts and extinguishes the reclose LED. Output contacts K2 close and actuate a lockout alarm 95 of FIG. 7. Also, output contacts K3 close and actuate a reclose fail alarm 97. Correspondingly, a lockout LED 99 and Reclose Fail LED 101 of FIG. 8 are illuminated. Reclose fail time is established by a pair of thumbwheels 103.

Detailed Description Text (29):
The front panel programmable reclose fail time set by thumbwheels 103 limits the duration of the reclose command at relay contacts K1 and LED 93. Initiated at the onset of a reclose command output signal, the reclose fail timing function compares the reclose fail time setting to the time the reclose command signal is present. If the set time on thumbwheels 103 is exceeded before the breaker closes, the relay immediately goes to lockout, the reclose fail output contact K3 is closed, and the reclose fail indicator 101 and lockout LED 99 illuminate. The reclose fail setting is adjustable in 0.1 second increments from 0.1 to 9.9 seconds. Omitting a reclose fail jumper input in FIG. 7 or setting reclose fail time thumbwheels 103 to 00 inhibits the reclose fail timer and causes the reclose command signal to continue as long as the breaker remains open.

Detailed Description Text (30):
However, if the breaker CB does close within the Reclose Fail Time, alarms 95 and 97 and LEDs 99 and 101 are not energized. Instead, the reclosing relay 61 now deenergizes output K1 and LED 93 and proceeds in its operations to wait until the breaker CB is tripped open or for a set-table period called Reset Time, which ever is less. (The reset timing function is also initiated during an initial power-up sequence when breaker CB is closed.) Reset Time is established by a pair of thumbwheels 105. The Reset Time setting is adjustable from 10 to 1000 seconds in 10 second increments and a setting of 00 corresponds to a 1000 second reset time. If the breaker CB remains closed for the entire Reset Time, the reclosing relay 61 automatically resets itself, clears the panel LEDs, and turns on RESET LED 91. Then if the breaker CB is tripped later on, the reclosing relay 61 starts with the instantaneous reclose attempt again.

Detailed Description Text (31):
If the breaker CB is tripped open before the Reset Time elapses, reclosing relay 61 does not reset. Instead, reclosing relay 61 proceeds to the first time delayed reclose attempt and begins timing a first reclose time delay TD1 established and indicated by three thumbwheels 109 in the range 0.1 second to 99.9 seconds. When time delay TD1 times out, output K1 closes, Reclose Output Energize LED 93 is turned on and another LED 111 is turned to display the first time delayed reclose. The reclose fail time begins to run as described above. Assuming the breaker CB

closes, LED 93 is turned off, the reclose output is de-energized and the reset time begins to run as also described above. If one or more subsequent trips occur, further status LEDs 113 and 115 are turned on for the second and third time delayed reclose attempts respectively. Time delays TD2 and TD3 for these time delayed attempts are respectively established and indicated by sets 121 and 123 of three thumbwheels each.

Detailed Description Text (33):
As discussed above, the three reclose time delays TD1, TD2 and TD3 are provided on thumbwheel switches 109, 121 and 123 for the second, third and fourth reclose attempts. The thumbwheels are individually adjustable in 0.1 second increments from 0.1 to 99.9 seconds. The number of reclosing attempts before lockout is front panel programmable. Setting any of the reclosure time delays to 000 produces lockout when that reclosing attempt is reached in the sequence. If the circuit breaker CB opens during the Reset Time after the first, second or third reclose attempt, the reclosing relay 61 proceeds to the next reclosing attempt, which is a time delayed attempt. Upon completion of the respective reclose time delay, the Reclose output relay K1 and LED 93 are energized and remain on for the length of the reclose fail time setting on thumbwheels 103 or until the breaker closes, whichever is less. The four STATUS LEDs 94, 111, 113 and 115 are illuminated in turn to indicate progression of reclosing sequence. The STATUS LEDs are extinguished on actuation of a front panel reset switch 151. The information of these LEDs is latched in the sense that if an attempt has been made the corresponding LED will remain lit until extinguished by actuation of front panel reset switch 151.

Detailed Description Text (38):
(3) reclose failure occurs, or

Detailed Description Text (41):
The reclosing relay 61 of FIG. 8 provides flexibility of response to minimize inconvenience and system damage when a fault occurs. Contact inputs are provided to select a reclosing sequence, modify a programmed sequence, or cause the relay to go to lockout. These contacts are suitably provided directly from supervisory control, and protection circuits (not shown) external to the reclosing relay 61. For system coordination, the reclosing relay performs automatic system control through outputs K1-K7.

Detailed Description Text (46):
Jumpers are connected at inputs designated Reclose Fail, Max Cycle Time, and Memory Initiate in FIG. 7 to trigger the corresponding reclosing relay 61 features. In Reclose Fail the reclosing relay can determine whether or not the circuit breaker is responding to a reclose command. In Max Cycle Time an overall time limit for the reclosing cycle is established. In Memory Initiate, the reclosing relay 61 continues from an identified operation in the reclosing sequence after a temporary loss of operating power from transformer 65 by "remembering" that operation which was being performed in the reclosing cycle when power was lost.

Detailed Description Text (50):
Another three output contacts of the reclosing relay 61 are used to control alarms: Lockout alarm contacts K2, Reclose Fail alarm contacts K3 and Relay Fail alarm contacts K6. A Relay Fail alarm 136 is energized if there is a loss of power to the reclosing relay 61 or a microprocessor failure therein. A Relay Fail LED 137 in FIG. 8 is also turned on at such time. The Reclose Fail alarm 97 and the Lockout alarm 95 have been described hereinabove.

Detailed Description Text (58):
In FIG. 10 reclosing relay 61 has a 80C39 CMOS (complementary metal oxide semiconductor) microcomputer 201 that has an internal central processing unit (CPU) and random access memory (RAM). An 8 bit bus 211 connects microcomputer 201 to the output of an 8 bit inverting buffer 213 which is connected to the five

optoisolators 73 for the 52b, RI, IRB, DTL and PRI inputs. The three jumper inputs for Reclose Fail, Max Cycle Time and Memory Initiate (MI) together with the optoisolators 73 supply 8 inputs to buffer 213.

Detailed Description Text (62):
Microcomputer 201 collects the thumbwheel information by addressing input lines 1-8 of thumbwheel switches 81 with respective single high bits and latching the switch 81 output on lines 235 into latch 241 with a command WR/ to latch enable pin LE/. Outputs 1Q-8Q are tristate outputs that float electrically until a chip-enable OR-gate 245 supplies an output control signal to pin OC/ to output the latch contents onto data bus 211. OR-gate 245 responds to address bit A0 low and read output RD/ low. Microcomputer 201 is programmed in a conventional manner to segregate and interpret the thumbwheel information as two digit or three digit numbers as indicated in FIG. 8. Thumbwheels 103, 109, 121, and 123 are interpreted as having decimal tenths for the least significant digit. The numerals displayed on thumbwheels 105 are interpreted as representing a number that is ten times larger, see the legend "x10" in FIG. 8.

Detailed Description Text (68):
In normal operation the microcomputer 201 randomly outputs pulses at intervals that have a reasonably predictable arithmetic mean. If these pulses are disrupted, the program monitor circuit 301 discontinues microcomputer operation, illuminates Relay Fail LED 137 through a first output of latch 271 and otherwise extinguishes the panel LEDs by forcing the rest of the latches 271 and 291 to high impedance by a high through an Output Disable line OD. (A resistor 249 otherwise holds line OD low). (A resistor 249 otherwise holds line OD low.) This causes all output contacts K1-K7, including the normally closed contacts K5 and K6, to assume their normal states. If the Output Disable is the result of something other than hardware failure, it is suitably remedied by manually interrupting operating power and turning it back on.

Detailed Description Text (81):
Only one of time values RECTD (Reclose Time Delay) of RSTTIM (Reset time) is stored in NOVRAM in a given instance, according to which timer is enabled as indicated by TIMEN byte. The timer value is the time remaining until timeout, and only the two most significant BCD digits are stored as the 8 bits. Total Duty Cycle Time (Maximum Cycle Time) TDCTIM is a separate byte from RECTD/RESTTIM, and TDCTIM holds the timer value for the time remaining until timeout. A Reclose Fail Time RCFLTM remaining until timeout is also stored, in FIG. 12. If both digits are zero, then a time delay of zero is assumed, except for TDCTIM and RSTTIM where digits of "9" are assumed. Thus, microcomputer 201 has an operation in the reclosing sequence that comprises timing a predetermined time interval and is responsive to an occurrence of the second signal (e.g. INT/) for storing a value representing a time period remaining in the predetermined time interval when the interval is being timed and the second signal occurs. The predetermined time interval can be a reclose time delay, a reset time interval after reclosure, a maximum cycle time for the reclosing relay, or a reclose fail time, for instance.

Detailed Description Text (94):
Microcomputer 201 thereupon jumps to a predetermined hardware location and begins executing a power loss interrupt routine. A test is made in a step 515 to determine whether the reclosing relay 61 is in a reclosing enabled condition as indicated by a "one" in the Reclose Enable bit REC EN of the loop state LPSTAT byte of FIG. 11. This condition typically signifies that reclosing relay 61 has left Reset and is going through a reclosing sequence. If so, operations proceed to a step 571 to turn off the Status LEDs 94, 111, 113, 115 and 135. Also, in step 517, the bytes LPSTAT, ATTCNT, TIMEN, TIMOUT, OUTLED and OUTCON of FIG. 11 are stored in nonvolatile memory 311 of FIGS. 10 and 12. In addition, the time remaining in pertinent timer registers is stored in memory 311. These include Reclose Time Delay RECTD, Reclose Fail Time RCFLTM and Reset Time RSTTIM, depending on which timer is appropriate.

Also, Total Duty Cycle Time (TDCTIM) is stored in memory 311, which time is the time remaining in the maximum cycle time permitted to the relay.

Detailed Description Text (101):
If reset or lockout in step 615 then a branch is made to step 609 to destroy the stored bytes. If there was neither reset nor lockout in step 615, then operations proceed to a step 617 where a test is made to determine whether the reclosing relay was either in a normal reclose sequence or a pilot reclose sequence (REC EN or PI EN=1 in LPSTAT). If the relay was not in either sequence, then operations branch to step 609 to destroy the bytes in memory 311. If the relay was in either sequence, then operations proceed to a step 619 where microcomputer 201 energizes relay K6 so that normally closed contacts thereof become open and the associated LED 137 extinguishes to remove any Relay Fail indication.

Detailed Description Text (110):
Operations in reset block 683 commence with Begin Reset State point 691 and go to a step 693 to light the RESET LED 91, disable BLTC to permit load tap changer operation by deenergizing relay K5, clear LPSTAT and ATTCNT and set the reset bit RST therein and in ATTCNT, turn off lockout relay K2 and lockout LED 99, turn off Max Cycle LED 133, energize the normally closed Relay Fail relay to open its contacts K6, and turn off Relay Fail LED 137.

Detailed Description Text (117):
In FIG. 19 operations at point D proceed to a step 751 where the pertinent reclose time delay LED 94, 111, 113 or 115 is lighted in addition to any of them which may already be lighted. Then a step 753 tests for pilot enable in LPSTAT. If there is no pilot enable, then operations proceed to a step 755 to close the reclose output contacts K1 and turn on reclose output LED 93. Then in a step 757, the Reclose Fail Time value derived from thumbwheels 103 is tested for "00". If not "00" then a step 759 starts the reclose fail timer by setting bit RF in byte TIMEN of FIG. 11. Then a step 761 tests 52b closed (CB open) and if 52b is still closed because CB has not actually closed yet in response to the reclosing command of step 755, then a step 763 tests for reclose fail timer timeout. If it is not timed out a loop is executed through check subroutine in a step 765 and a lockout flag test step 767 and back to step 761 until either the breaker closes (step 761) or the reclose fail timer times out (step 763) or there is a reason to go to lockout point E because of the lockout flag (step 767). If the breaker CB closes then a branch is made from step 761 to a step 769 to deenergize the reclose output K1 and LED 93 and the pilot output K7. Point A is now reached, and operations return to Reset Timing and Lockout routine of FIG. 16. However, if the Reclose Fail timer times out before the breaker CB closes, then a branch is made from step 763 to a step 771 to energize the reclose fail contact K3 and LED 101, and deenergize the reclose output K1 and LED 93 whereupon point E and lockout step 663 of FIG. 16 are reached.

Detailed Description Text (118):
If in step 753 of FIG. 19 there is a pilot enable PI IN=1 in LPSTAT, then the pilot output K7 and LED 135 are energized in a step 773 and operations proceed to a step 775 to test the state of the breaker CB. Also, if the Reclose Fail time thumbwheels 103 are "00" in step 757 a branch to step 775 is also made. If at such time, the breaker is closed (52b open) then a branch is made to step 769 to de-energize the reclose and pilot reclose outputs and to go back to Reset state FIG. 16. However, if the breaker is open (52b closed), then a loop is made through a check subroutine step 777 and a lockout flag F0 test 779 and back to step 775 in order to continue the reclose command either through the K1 or K7 contact as the case may be until the breaker finally closes or lockout is reached by other means from step 779.

Detailed Description Paragraph Table (3):
TABLE II _____ LPSTAT bits (only one of bits 1-5 is "1" at any one time) PWR INT one if power has been interrupted; stored in NOVRAM when power goes down. Bit 6 Unused. REC EN one when a valid reclosing sequence has

h e b b g e e e f c e e e ge

been initiated and stays 1 until the sequence is terminated. REC EN is not a 1 in reset or pilot enable or lockout or power up. RST one in the Reset state and zero in initial power up phase, or reclosing sequence or lockout. LO one in lockout. PWR UP one in initial power up sequence. PI EN one when a valid pilot sequence is initiated and the reclosing relay comes off reset. ATTCNT (Attempt counter) Bit 7 TDC Carry set to one if "000" on Max Cycle Time thumbwheels. Total Duty Cycle is 1000 seconds. Bit 6 Reset Carry set to one if "00" on Reset Time thumbwheels. Reset Time is 1000 seconds. Bit 0 Reset state. Bit 1 Instantaneous trip set to 1 on inst. trip. A "1" is shifted left from bit 0. Bits 2,3,4 Have a "1" shifted through them if and when the relay reaches their respective 1TD, 2TD, and 3TD reclose time delays. If relay is to lock out upon reaching 2TD, for example, then 2TD thumbwheels are set to "000" and the 2TD bit is preset to a 1, and then when 2TD is reached, the microcomputer sees that 2TD is already 1. Bit 5 When "1" is shifted into bit 5, recloses are exhausted, and relay goes to lockout. TIMEN Control Byte Identifying Enabled Timers 3TD, 2TD, 1TD one for Third, Second or First Time Delayed Reclose Timer enabled RF one if Reclose Fail Timer is enabled. If any of 3TD-1TD are enabled then RF is a 0. RST One if Reset Timer is enabled. Only one of the groups (A) RST, (B) RF, and (C) 1TD 2TD, 3TD is a 1 at any given time. TDC One if Total Duty Cycle Timer (Max Cycle Timer) is enabled. TIMOUT Control Byte Identifying Timed Out Timers. Timer identified same as in TIMEN. If a timer is timed out there is a 1 in the corresponding bit position, otherwise zero. OUTLED Control Byte of Panel LEDs one is set for each of 8 LEDs which are lighted, identified as on FIG. 11 map. OUTCON Control Byte of Output Contacts (Positive logic) In every case OUTCON 1 bit signifies an energized output relay whether is it is normally open or nor- mally closed type. LTC is "1" if BLTC is enabled.

CLAIMS:

12. A reclosing relay as set forth in claim 1 wherein the predetermined time interval is a reclose fail time.

L1: Entry 80 of 225 File: USPT Aug 28, 2001

DOCUMENT-IDENTIFIER: US 6282699 B1
** See image for Certificate of Correction **
TITLE: Code node for a graphical programming system which invokes execution of textual code

Drawing Description Text (4):
FIG. 1A illustrates an industrial automation system according to one embodiment of the present invention;

Detailed Description Text (17):
FIG. 1A illustrates an industrial automation system 160. The industrial automation system 160 is similar to the instrumentation or test and measurement system 100 shown in FIG. 1. Elements which are similar or identical to elements in FIG. 1 have the same reference numerals for convenience. The system 160 comprises a computer 102 which connects to one or more devices or instruments. The computer 102 comprises a CPU, a display screen, memory, and one or more input devices such as a mouse or keyboard as shown. The computer 102 connects through the one or more devices to a process or device 150 to perform an automation function, such as MMI (Man Machine Interface), SCADA (Supervisory Control and Data Acquisition), portable or distributed data acquisition, process control, advanced analysis, or other control.

Detailed Description Text (27):
The host bus 202 is coupled to an expansion or input/output bus 210 by means of a bus controller 208 or bus bridge logic. The expansion bus 210 is preferably the PCI Peripheral Component Interconnect) expansion bus, although other bus types can be used. The expansion bus 210 includes slots for various devices such as the data acquisition board 114 (of FIG. 1), the GPIB interface card 122 which provides a GPIB bus interface for coupling to the GPIB instrument 112 (of FIG. 1), and a VXI or MXI bus card 186 for coupling to the VXI chassis 116 for receiving VXI instruments.

Detailed Description Text (90):
A type conflict error will be returned if data conversion between the graphical programming system and the prograrn server fails. The implementation includes straight forward, conversion, atray dimension change and extraction at the OLE variant level. Existing OLE variant functions are preferably used for the script node. The DLL includes two data conversion functions:

Detailed Description Paragraph Table (2):
Error Code Error Code Message Description 1046 edScriptCantInitServer LabVIEW failed to initiate a new session with the server. 1047 edScriptCantSetValue LabVIEW failed to set the value of a variable to the server. 1048 edScriptCantGetValue LabVIEW failed to retrieve the value of a variable from the server. 1049 edScriptCantSetScript LabVIEW failed to set a script to the server. 1050 edScriptExecError LabVIEW encountered an execution problem. The server returns a string to report the problem.